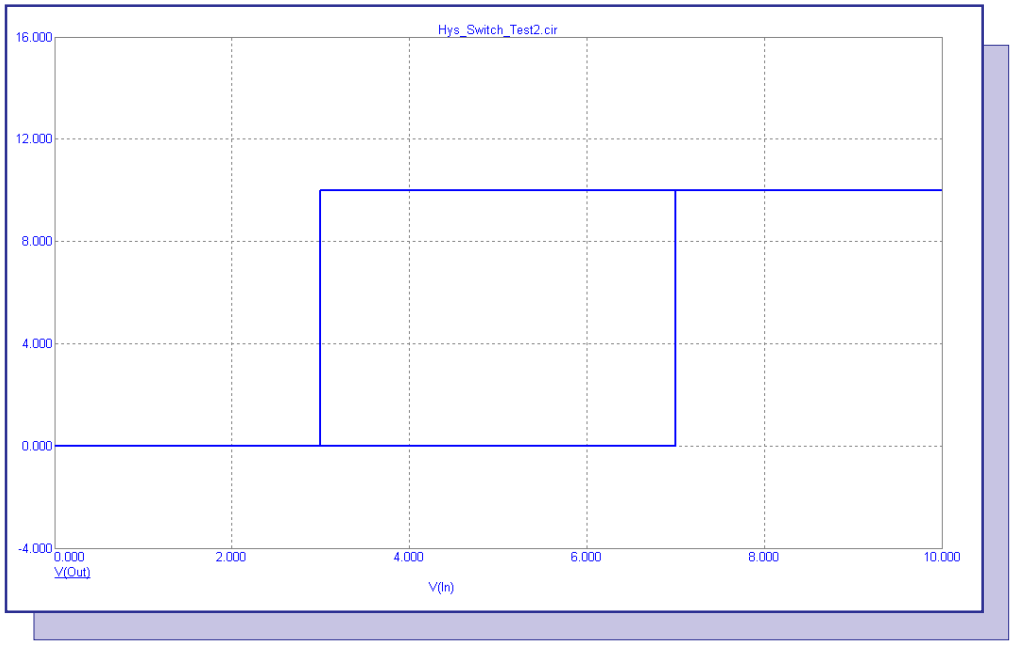
spectrum news

Applications for Micro-Cap™ Users

Winter 2003

News



Hysteresis Switch Macro

Featuring:

- Creating A Digital I/O Interface Model
- Modifying Component Icons In The Toolbar
- Hysteresis Switch Macro

News In Preview

This newsletter's Q and A section describes how to create a noiseless resistor and what to do when a .TOP file can't be found. The Easily Overlooked Features section describes the analysis plot title variables that are available within Micro-Cap.

The first article describes the process of creating a new digital I/O interface model for the 74LV-A family.

The second article describes how to modify or add component icons to the main toolbar.

The third article describes a new switch macro that models a hysteresis input.

Contents

Book Recommendations

General SPICE

• *Computer-Aided Circuit Analysis Using SPICE*, Walter Banzhaf, Prentice Hall 1989. ISBN# 0-13-162579-9

• *Macromodeling with SPICE*, Connelly and Choi, Prentice Hall 1992. ISBN# 0-13-544941-3

• *Inside SPICE-Overcoming the Obstacles of Circuit Simulation*, Ron Kielkowski, McGraw-Hill, First Edition, 1993. ISBN# 0-07-911525-X

• *The SPICE Book,* Andrei Vladimirescu, John Wiley & Sons, Inc., First Edition, 1994. ISBN# 0-471-60926-9

MOSFET Modeling

• *MOSFET Models for SPICE Simulation, William Liu, Including BSIM3v3 and BSIM4*, Wiley-Interscience, First Edition, ISBN# 0-471-39697-4

VLSI Design

• *Introduction to VLSI Circuits and Systems,* John P. Uyemura, John Wiley & Sons Inc, First Edition, 2002 ISBN# 0-471-12704-3

Micro-Cap - German

• *Schaltungen erfolgreich simulieren mit Micro-Cap V,* Walter Gunther, Franzis', First Edition, 1997. ISBN# 3-7723-4662-6

Micro-Cap - Finnish

• *Elektroniikkasimulaattori,* Timo Haiko, Werner Soderstrom Osakeyhtio, 2002. ISBN# ISBN 951-0-25672-2

Design

• *Microelectronic CircuitsHigh Performance Audio Power Amplifiers,* Ben Duncan, Newnes, First Edition, 1996. ISBN# 0-7506-2629-1

• *Microelectronic Circuits.,* Adel Sedra, Kenneth Smith, Fourth Edition, Oxford, 1998

High Power Electronics

• *Power Electronics,* Mohan, Undeland, Robbins, Second Edition, 1995. ISBN# 0-471-58408-8

• *Modern Power Electronics,* Trzynadlowski, 1998. ISBN# 0-471-15303-6

Switched-Mode Power Supply Simulation

• *SMPS Simulation with SPICE 3,* Steven M. Sandler, McGraw Hill, First Edition, 1997. ISBN# 0-07-913227-8

• *Switch-Mode Power Supply SPICE Simulation Cookbook*, Christophe Basso, McGraw-Hill 2001. This book describes many of the SMPS models supplied with Micro-Cap.

Micro-Cap Questions and Answers

Question: How do I create a noiseless resistor?

Answer: In the model statement for a resistor, there is a parameter called NM that is a noise multiplier. To edit the NM parameter in a schematic, go to the Attribute dialog box of the resistor. Define the MODEL attribute if it is not already defined. Highlight the MODEL attribute. Once the model name has been defined and the attribute is highlighted, the parameter fields at the bottom of the dialog box will become active and available for editing. NM will be in the list. This parameter multiplies the noise that the resistor produces by its defined value. Setting NM to 0 creates a noiseless resistor.

Question: I just received a circuit from another user and when I go into transient analysis and try to run, I get an error stating that Micro-Cap can't find a .TOP file. How do I resolve this error?

Answer: The .TOP file is created by the State Variables Editor and is used to store the State Variables that initialize the start of the transient simulation. You would need to get this file from the other user, or in the Transient Analysis Limits dialog box, you can change the State Variables option to Zero or Leave. Changing the State Variables option will most likely give you a different simulation result than what the other user intended since you will be beginning the transient simulation at a different initial point. Whenever the State Variables option is set to Read, there must be a corresponding .TOP file present.

Easily Overlooked Features

This section is designed to highlight one or two features per issue that may be overlooked because they are not made visually obvious with a toolbar button.

Analysis Plot Title Variables
The Analysis Properties dialog box contains a Title field in its Plot page that lets a user define the title of the analysis plot. Typically, the Auto checkbox is enabled and Micro-Cap automatically creates the title from the circuit name and the analysis run details. When the Auto checkbox is disabled, the user has complete control of the analysis title. Micro-Cap contains some generic variables that give the user greater flexibility in defining a title. They are as follows:

$MCCASE - This prints the number of the Monte Carlo case that is currently running or that the cursor is on.
$CASE - This prints the Monte Carlo case that is currently running in the format: 'Case=#'.
$TEMPLOW - This prints the value of the lowest temperature.
$TEMPHIGH - This prints the value of the highest temperature.
$TEMPCURRENT - This prints the temperature of the analysis that is currently running or that the cursor is on.
$TEMPERATURE - This prints the temperature range in the format 'Temperature=<value>" or "Temperature=<value1>....<valuen>".
$STEPLOW# - This prints the low value of the specified number parameter. For example, $STEPLOW1 will print the low for parameter 1.
$STEPHIGH# - This prints the high value of the specified number parameter. For example, $STEPHIGH2 will print the high for parameter 2.
$STEPCURRENT# - This prints the value of the specified number parameter that is currently running or that the cursor is on.
$STEPNAME# - This prints the name of the specified number parameter. For example, $STEPNAME1 will print the name of parameter 1.
$STEPPING# - This prints the range of the specified number parameter. For example if parameter one is a resistor named R1 being stepped from 50 to 100. $STEPPING1 will print 'R1=50..100'.
$STEPPING - This prints the name and range of all parameters being stepped.

You can also use .define statements in the title. For example, if you have a statement in the schematic such as:

.define Title My Circuit

you can reference this in the title field by stating '$Title$'.

Many of the variables from the title block of the schematic are also available such as: $MC, $DATE, $TIME, $USER, $COMPANY, $NAME, and $NAMEEXT.

Creating A Digital I/O Interface Model

Digital I/O models capture the electrical information common to the IC technology and circuit techniques used to design and build them. A typical digital family will only have a few I/O models. The only difference in the I/O models within a digital family is to account for the different circuits employed at the input or output such as open-collector outputs or Schmitt-trigger inputs. The I/O models provide the information necessary to determine the output strength when devices are wire-ored together, and to create the interface circuits when the digital part is connected to an analog part. This article will describe the steps taken to create an I/O interface for the 74LV-A low voltage logic family at its typical power supply voltage of 3.3V.

Power Supply Subcircuit

The digital power supply subcircuit defines the default power supply for the logic family when the supply is not specified in a schematic. This subcircuit is called whenever an AtoD or DtoA interface is required. Multiple logic families can use the same power supply subcircuit if it is applicable. For the 74LV-A family, the nominal voltage supply for the VCC pin is 3.3V. The subcircuit below defines the power supply.

```
.subckt DIGIFPWR_3V AGND
+  optional: DPWR_3V=$G_DPWR_3V DGND_3V=$G_DGND_3V
+   params: VOLTAGE=3.3 REFERENCE=0
V1 DPWR_3V AGND {VOLTAGE}
R1 DPWR_3V AGND 1E9
V2 DGND_3V AGND {REFERENCE}
R2 DGND_3V AGND 1E9
R3 AGND 0 1m
.ends
```

The subcircuit basically consists of two batteries with a large resistor in parallel with each. The batteries are defined by the VOLTAGE and REFERENCE parameters, which in this case, have been defined as 3.3V and 0V respectively. The optional nodes, DPWR_3V and DGND_3V, define the power and ground node names that will be used throughout the I/O model and in components that reference this I/O model.

Digital Input Device (N Device) Model Statement

The digital input device is the device within the interface that converts a digital output node to its analog equivalent. It does the conversion by translating the digital states to impedance changes on the analog side. Two resistors (RLO and RHI) are placed in a voltage divider configuration between the power and ground nodes of the digital device. These resistors determine the equivalent analog voltage of the digital output. The model statement for the N device defines the values of the resistors for each digital state, and the switching time between the old resistance and the new resistance when a state change occurs. The model statement for the standard N device in the 74LV-A family is:

```
.model DIN74LV-A dinput (
+  s0name="0"  s0tsw=3.4n  s0rlo=31.9   s0rhi=494.5   ;@30ohms, .2V
+  s1name="1"  s1tsw=3.4n  s1rlo=578.2   s1rhi=37.3   ;@35 ohms, 3.1V
+  s2name="F"  s2tsw=3.4n  s2rlo=58.1  s2rhi=73.2   ;@32.4 ohms, 1.46V
+  s3name="R"  s3tsw=3.4n  s3rlo=58.1  s3rhi=73.2   ;@32.4 ohms, 1.46V
+  s4name="X"  s4tsw=3.4n  s4rlo=58.1  s4rhi=73.2   ;@32.4 ohms, 1.46V
+  s5name="Z"  s5tsw=3.4n  s5rlo=1Meg  s5rhi=1Meg)
```

The N device model statement defines three parameters for each state: the switching time (tsw), the low resistance (rlo), and the high resistance (rhi). The switching time defines the amount of time it takes for the resistors to transition to their new value for the state. The switching times should be close to the typical propagation delay for the family. The main I/O model has parameters that compensate for these switching times, so that the resistance values reach their new value at approximately the same time as the state changes at the output. A 0-R-1 transition will produce a 6.8ns switching time for this model.

The resistance values for each state are determined by the V-I curves for the family. For the 0 state, the slope of the VOL vs IOL curve is taken to obtain a resistance (RSL). The RSL resistance is then used to calculate the RLO and RHI resistors in the model statement through the two following equations:

VO = (VPWR*RLO)/(RLO + RHI)
RSL = (RLO*RHI)/(RLO + RHI)

VPWR is the power supply for the family which in this case is 3.3V. VO is the typical low state output voltage at a power supply of 3.3V which is .2V for this family. RSL was determined to be 30 ohms from the VOL vs IOL curve, so the resulting resistances for the 0 state are RLO=31.9 and RHI=494.5. For the 1 state, the same equations are used except that the RSL is determined by the slope of the VOH vs IOH curve, and VO is the typical high state output voltage which is 3.1V for this family. With the RSL resistance measured at 35 ohms, the resistances for the 1 state are calculated at RLO=578.2 and RHI=37.3.

For the F, R, and X states, the above equations are also used. These three states will be arbitrarily represented as a midpoint between the 0 and 1 states. The RSL resistance for these states is determined by taking the square root of the product of the RSL resistances determined for the 0 and 1 state as follows:

RSL = SQRT(RSL(0) * RSL(1))

The VO voltage is defined as the voltage exactly halfway between the minimum high output voltage and the maximum low output voltage. For the 74LV-A family, the RSL comes out to 32.4 ohms and the output voltage is determined to be 1.46V. These values produce resistances of RLO=58.1 and RHI=73.2.

For the Z state, the RHI and RLO parameters have been arbitrarily assigned the value of 1Meg to represent the high impedance of the state, and the switching time is set to the same value as the F, R, and X states.

DtoA Interface Subcircuit

The DtoA interface subcircuit is the actual component that is placed between a digital output and an analog component internally when an analysis is entered. For the 74LV-A family, the subcircuit is as follows:

```
.subckt DTOA_LV-A D A DPWR_3V DGND_3V
+  params: CAPACITANCE=0 DRVH=0 DRVL=0
N1 A DGND_3V DPWR_3V DIN74LV-A DGTLNET=D IO_LV-A
CLOAD A DGND_3V {CAPACITANCE+.1p}
.ends
```


The DtoA subcircuit consists of only two components, an N device, referencing the model statement just created, and a capacitor. The power and ground nodes throughout the subcircuit are given the same name as the power and ground nodes in the power supply subcircuit. The I/O model specification for the N device is defined with the name of the full I/O model, IO_LV-A, that will be created further along in this article. The DRVH and DRVL parameters are the high state and low state impedances used to determine output strength. The CAPACITANCE parameter is used to increase the propagation delay through the device to account for excessive capacitive loading on the node caused by high fan-out. These parameters will be overwritten by the DRVH, DRVL, and OUTLD parameters available in the IO_LV-A model, so they are set to 0 for the subcircuit. The schematic equivalent of the DtoA subcircuit interface appears in Figure 1.

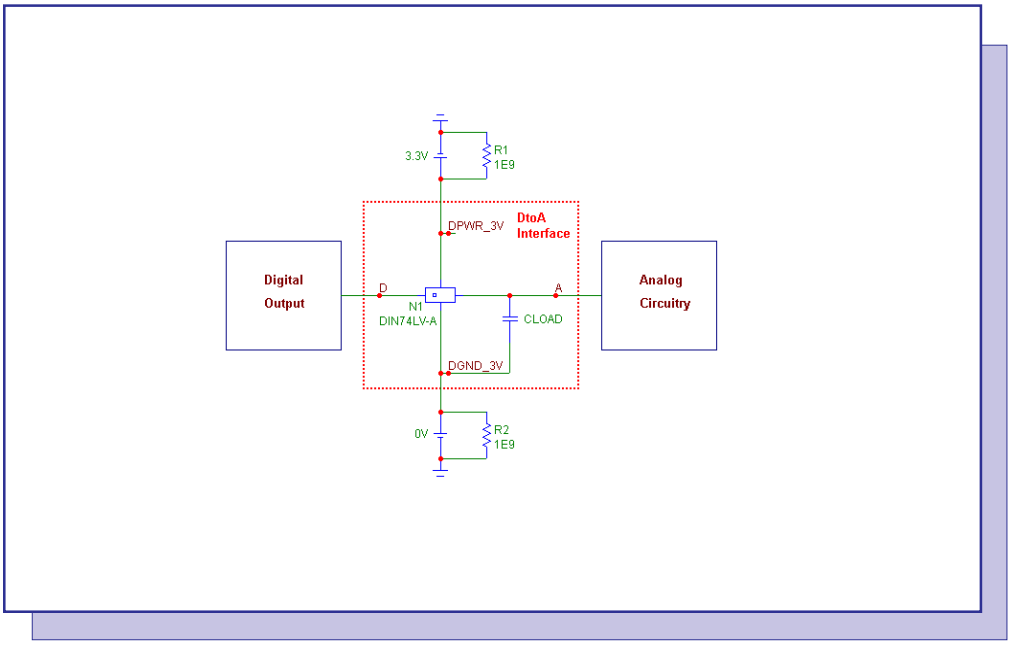


Fig. 1 - DtoA Schematic Equivalent

Digital Output Device (O Device) Model Statements

The digital output device is the component that converts an analog voltage into its equivalent digital state for when an analog node is connected to a digital input. It does the conversion by assigning voltage ranges to the digital states. If the analog input voltage falls within a range, the output will be the corresponding digital state. These voltage ranges are defined in the model statement for the O device. The 74LV-A family will have two O device model statements. One model will contain all the intermediate states such as R, F, and X along with the 0 and 1 states, and the other will be a simplified model that contains only the 0 and 1 states. This is typical of all of the families that are included with Micro-Cap. The model that is actually used in simulation is dependent on the Global Setting DIGIOLVL parameter which specifies which of the four DtoA and AtoD subcircuit interfaces to use. The two O model statements for the 74LV-A family are:

```
.model DO74LV-A_NX doutput (
+  s0name="0"  s0vlo=-.5  s0vhi=1.65
+  s1name="1"  s1vlo=1.65  s1vhi=7)
```

```
.model DO74LV-A doutput (
+  s0name="X"  s0vlo=.8    s0vhi=2
+  s1name="1"  s1vlo=2     s1vhi=7
+  s2name="F"  s2vlo=1.6   s2vhi=2
+  s3name="F"  s3vlo=.8    s3vhi=1.7
+  s4name="X"  s4vlo=.8    s4vhi=2
+  s5name="0"  s5vlo=-.5   s5vhi=.8
+  s6name="R"  s6vlo=.8    s6vhi=1.7
+  s7name="R"  s7vlo=1.6   s7vhi=2)
```

To determine which range contains the input voltage level, a progressive search is employed. The search starts at the current state range. If the voltage is outside this range, it tries the next possible range. If it fails on the last specified range, it will wrap around to the first range again. If it fails all of the ranges, it will choose the range with the nearest voltage match.

The DO74LV-A model represents the more complex AtoD interface. The 1 state defined on the s1 line uses the high level input voltage as its low voltage and the maximum input voltage as its high voltage. The 0 state defined on the s5 line uses the minimum input voltage as its low voltage and the low level input voltage as its high voltage. The R, F, and X states are defined within the voltage range set by the low level input voltage and the high level input voltage. The order that the states are defined in is also important due to the nature of the progressive search. Typically, the first state defined should be an X (unknown) state. This is the range that the simulation will first test. If the input voltage at that point is between .8V and 2V, it doesn't know whether it should be at a 0 or 1 state and will produce a resulting X state. The next state was chosen to be a 1 state. Following the 1 state is a combination of F (fall), F, and X states. The logic behind this combination is that it forces the analog input to have a fairly smooth transition between the 1 and 0 state. If the input voltage ramps linearly down from 2.5V to .5V, the digital output will go from the 1 state, to the first F state, to the second F state, and then to the 0 state. In the simulation, the user will just see a 1-F-0 transition. If the input analog voltage were to oscillate on the way down such as going from 2.5V to 1.5V back up to 1.8V and then down to .5V, the digital output will go from the 1 state, to the first F state, to the second F state, to the following X state, and then to the 0 state. In the simulation, the user will see a 1-F-X-0 transition. The X state is present to show that oscillation around the input threshold voltage will produce an ambiguous situation. This is the reason the F state was divided into two separate ranges around the input threshold voltage. The 0, R (rise), and R combination as the final three states are defined with the same logic in mind. This combination wraps around to use the s0 X state as its unknown state in case of oscillation.

The DO74LV-A_NX model represents the simple AtoD interface. The 0 state range is defined between the minimum input voltage and the input threshold voltage, and the 1 state range is defined between the input threshold voltage and the maximum input voltage. The order of the states in this model is meaningless since there are only two voltage ranges to sample from.

AtoD Interface Subcircuits

The AtoD interface subcircuit is the actual component that is placed between an analog component and a digital input internally when an analysis is entered. Two AtoD subcircuits will be created for this model in order to take advantage of both of the digital output device model statements created in the previous section. For the 74LV-A family, the subcircuits are as follows:

```
.subckt ATOD_LV-A A D DPWR_3V DGND_3V
+  params: CAPACITANCE=0
O1 A DGND_3V DO74LV-A DGTLNET=D IO_LV-A
C1 A DGND_3V {CAPACITANCE+.1P}
D1 DGND_3V A D74
R1 A 1 170
C2 1 DGND_3V 1p
.ends

.subckt ATOD_LV-A_NX A D DPWR_3V DGND_3V
+  params: CAPACITANCE=0
O1 A DGND_3V DO74LV-A_NX DGTLNET=D IO_LV-A
C1 A DGND_3V {CAPACITANCE+.1P}
D1 DGND_3V A D74
R1 A 1 170
C2 1 DGND_3V 1p
.ends
```

The only differences in the two subcircuits are in the subcircuit name and in the model name that the O device references. This AtoD subcircuit consists of five components. The O device, referencing one of the model statements from the previous section, is the heart of the subcircuit and performs the AtoD conversion. The power and ground nodes throughout the subcircuit are given the same name as the power and ground nodes in the power supply subcircuit. The I/O model specification for the O device is defined with the name of the full I/O model, IO_LV-A, that will be created next. The CAPACITANCE parameter is used to increase the propagation delay through the device to account for excessive capacitive loading on the node caused by high fan-out and is modelled by the C1 capacitor in the subcircuit. This parameter will be overwritten

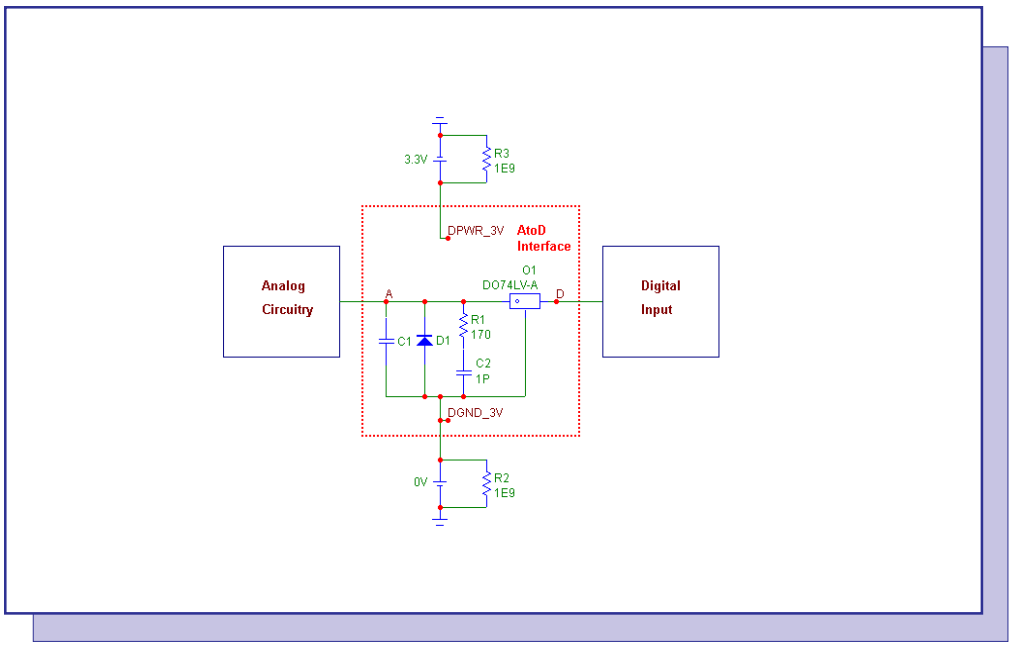


Fig. 2 - AtoD Schematic Equivalent

by the INLD parameter available in the IO_LV-A model, so it is set to 0 for the subcircuit. The rest of the components are used to model the typical analog input circuitry of the digital component. For the 74LV-A family, which is created through a CMOS process, the input is dominated by the ESD protection scheme which is modelled by the D1 diode, R1 resistor, and C2 capacitor. The 74LV-A family has no current paths to the power node in order to be able to interface directly with TTL devices, so the power node in the AtoD interface subcircuit will be left floating. The power node is still available as it is frequently used in many digital families, and it is displayed as unconnected in the schematic equivalent of the AtoD interface shown in Figure 2.

I/O Model Statement

The I/O model provides the information necessary to determine the output strength when devices are wire-ored together and to create the interface circuits when the digital part is connected to an analog part. The model brings together all of the subcircuits and models defined in the previous sections for use by a digital component. The I/O model statement for the 74LV-A family appears as follows:

```
.model IO_LV-A uio (
+  DRVH=130 DRVL=130
+  INLD=2.3p
+   ATOD1="ATOD_LV-A" ATOD2="ATOD_LV-A_NX"
+   ATOD3="ATOD_LV-A" ATOD4="ATOD_LV-A_NX"
+   DTOA1="DTOA_LV-A" DTOA2="DTOA_LV-A"
+   DTOA3="DTOA_LV-A" DTOA4="DTOA_LV-A"
+   TSWHL1=2.80n TSWHL2=2.80n
+   TSWHL3=2.80n TSWHL4=2.80n
+   TSWLH1=2.01n TSWLH2=2.01n
+   TSWLH3=2.01n TSWLH4=2.01n
+  DIGPOWER="DIGIFPWR_3V")
```

DRVH and DRVL are the high state and low state impedances used to determine the output strength. The output strength is used to resolve the output state when a digital output is connected to other digital outputs. For the 74LV-A family, the line drive impedance is defined as 130 ohms for both the high and low states.

The INLD parameter defines the input load capacitance. It is used to compute the optional loading delay through the device to account for excessive capacitive loading on the node caused by high fan-out. In this instance, a capacitance of 2.3pF was chosen by selecting an average input capacitance value from the products in the family.

The ATOD1 through ATOD4 parameters define the names of the analog to digital interface subcircuits that will be called when an analog component is connected to a digital input. The actual subcircuit that will be chosen for an analysis will be determined by the IO_LEVEL parameter within a component that references the I/O model or by the Global Setting parameter, DIGIOLVL. If the value of DIGIOLVL is set to 2, then the subcircuit defined by the ATOD2 parameter will be used. Note that the simpler AtoD models have been defined as levels 2 and 4, whereas the more complex models are defined with levels 1 and 3. The DTOA1 through DTOA4 parameters define the names of the digital to analog interface subcircuits that will be called when a digital output is connected to an analog component. These parameters act in the same manner as the ATOD parameters. Since only one DtoA model has been defined for the family, that model is specified for all four parameters.

The TSWLH1 through TSWLH4 and TSWHL1 through TSWHL4 define the switching times for the I/O model. The switching times are subtracted from the digital device's propagation delay on outputs which are connected to analog components. The purpose is to compensate for the time it takes the DtoA interface circuit to switch. By compensating in this way, the analog signal at the other side of the DtoA interface should reach the switching level just when the digital device does at the stated delay. If a switching time is greater than the device's stated delay, a delay of zero will be used. The IO_LEVEL parameter within a component or the DIGIOLVL Global Setting parameter also determines which of the four switching times it will use here also. Since the same DtoA subcircuit is used for all four cases in this family, the switching times will be the same for each level of a transition.

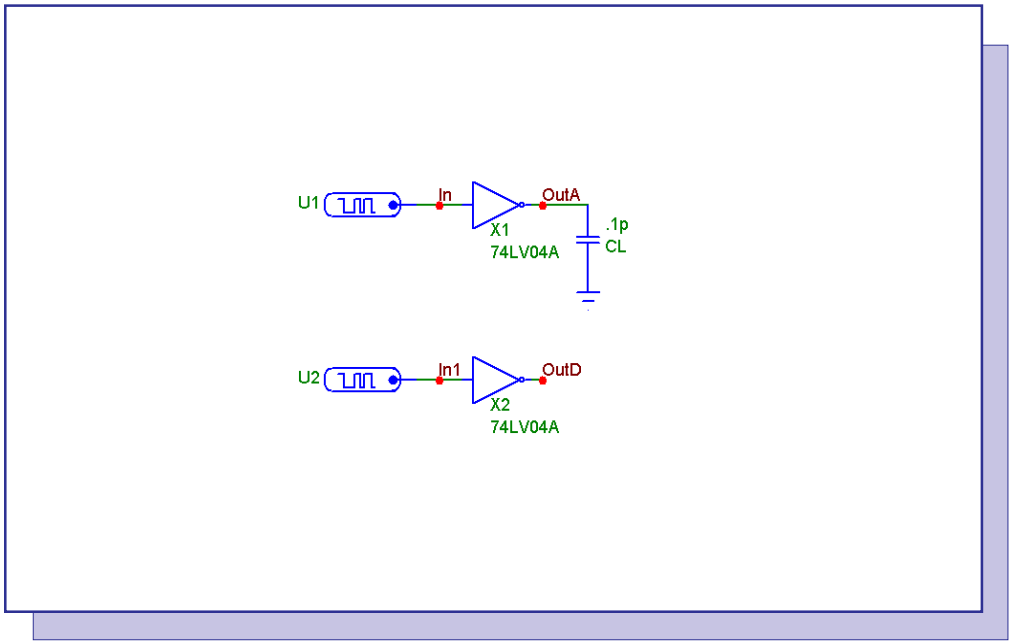


Fig. 3 - Switching Time Measurement Circuit

The switching time parameters in the I/O model are initially set to 0. To measure the switching times, a schematic similar to the one in Figure 3 may be used. The schematic consists of two separate circuits. The only difference between the two circuits is that the top one has a minimal load capacitance of .1pF whereas the bottom circuit has no load at all. The two digital stimulus sources start in the zero state, at 100ns transition to the one state, and at 200ns transition back to the zero state. These sources are fed into 74LV04A inverters which reference the I/O model that was just created. A transient analysis is run on this schematic with the results displayed in Figure 4. Three waveforms are plotted: D(In), D(OutD), and V(OutA). D(In) is the digital input waveform from one of the stimulus sources. D(OutD) is the digital output waveform of the inverter with no load, and V(OutA) is the output voltage waveform of the inverter with a capacitive load. The switching time is measured from the point that the no-load output makes its transition to when the capacitive load output reaches either the Vih or Vil value depending on the transition. For example, to measure the high to low switching time, one cursor is placed at the point where the D(OutD) waveform has a HL transition, and the other cursor is placed at the point where the analog output reaches its Vil voltage which in this case is .8V. The switching time is the time differential between these two points which comes out to 2.80ns for the 74LV-A model. Similarly,

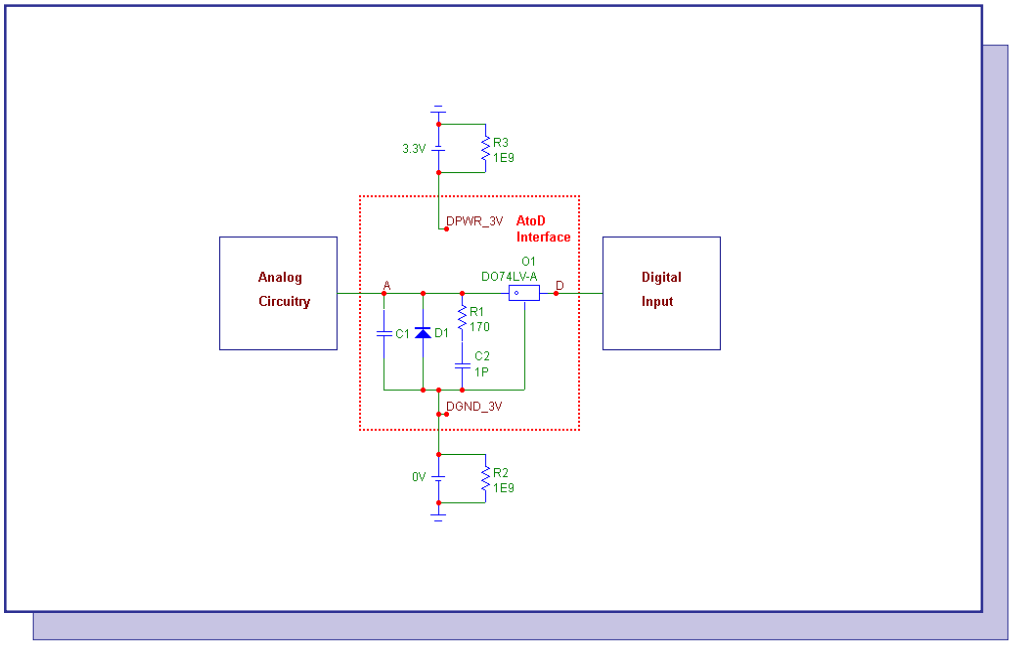


Fig. 4 - Switching Time Measurement Analysis

for the low to high switching time, one cursor is placed at the LH transition for D(OutD), and the other cursor is placed at the point where the analog output reaches its Vih voltage which is 2V for this family. The low to high switching time is measured at 2.01ns. The switching time parameters are then updated with these new values.

The DIGPOWER parameter specifies the name of the power supply subcircuit to be used when an AtoD or DtoA interface is required. The parameter is defined with the name of the DIGIFPWR_3V subcircuit that was created at the beginning of the article.

Example 74LV-A Family Digital Device

The 74LV04A inverter from the switching time measurement shows how the I/O model is referenced in an actual device.

```
.SUBCKT 74LV04A  1A  1Y
+     optional: DPWR_3V=$G_DPWR_3V DGND_3V=$G_DGND_3V
+     params: MNTYMXDLY=0 IO_LEVEL=0

U1 inv DPWR_3V DGND_3V
+     1A 1Y
+     DLY_LV04 IO_LV-A MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}

.model DLY_LV04 ugate (tplhTY=7.3ns tplhMX=10.6ns tphlTY=7.3ns tphlMX=10.6ns)

.ENDS  74LV04A
```

Note that the power and ground nodes (for both the optional nodes and the inverter supply nodes) use the same name as those in the digital power supply subcircuit referenced by the I/O model, and the inverter device within the subcircuit uses IO_LV-A as its I/O model name.

Modifying Component Icons In The Tool Bar

There are multiple ways in Micro-Cap to select a component for placement in a schematic. One can select a component by browsing through the Component menu, by clicking on a component name in one of the component palettes, by searching through the parts with the Find Component command, or by clicking on a component icon in the tool bar. Each of these methods have advantages, but for basic ease of use, the component icon method is considered the simplest. The default setup for the component icons tool bar is displayed in Figure 5 and can be found in the main tool bar for Micro-Cap.

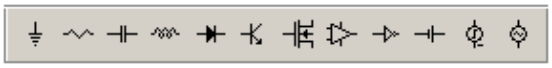


Fig. 5 - Default Component Icons

Each component icon is assigned to a single component. Clicking on one of these icons places the user in Component mode and ready to place the component that the icon is assigned to into the schematic. While the component menu and component palettes are controlled through the Component Editor, the component icons are modified through the Preferences dialog box. The page that controls the settings of the component icon tool bar can be found by clicking on the Options menu and choosing Preferences. In the Preferences dialog box, click on the Main Tool Bar tab. Highlight the Component item in the Tool Bar list, and the settings for the component tool bar are available for editing. The page should appear as in Figure 6.

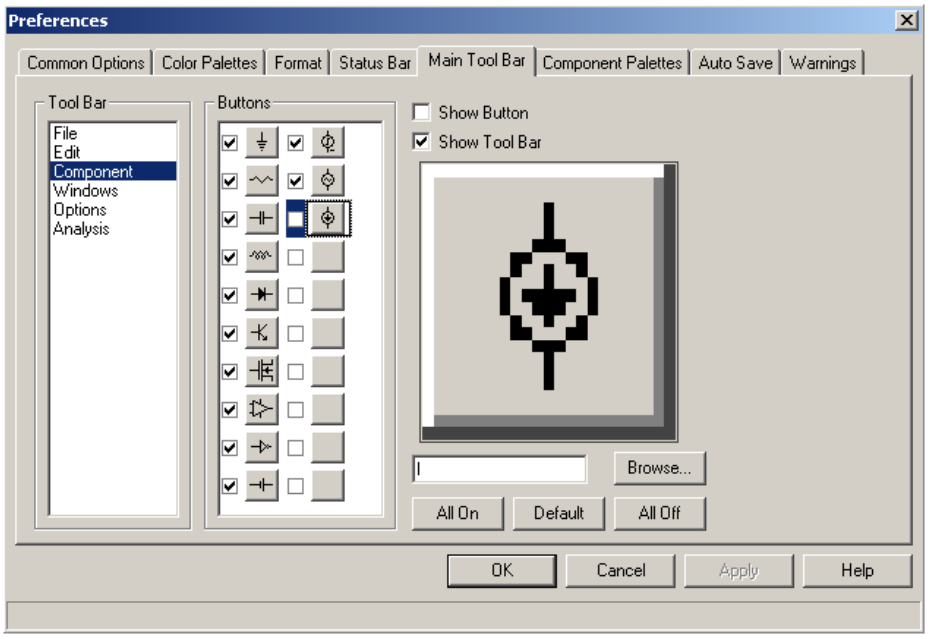


Fig. 6 - Main Tool Bar Panel in the Preferences Dialog Box

There are a total of 20 possible component icons that may be placed in the main tool bar. Micro-Cap comes with 12 of these icons predefined with such components as resistors, capacitors, inductors, and batteries. Any of these component icons may be edited by the user to suit their personal preferences.

The Main Tool Bar page for the component tool bar consists of six elements. The Buttons section shows all of the possible icons that are available to place in the main tool bar. A checkbox next to each icon lets the user display or hide that individual button. The Show Button checkbox performs the same operation for the selected button. The Show Tool Bar checkbox will display or hide the entire component tool bar. Below these two checkboxes is the Draw Button area. This area lets the user modify or create their own graphic for the selected component icon. Clicking on a pixel will toggle that pixel's color between gray and black. Below the Draw Button is the text field that assigns a specific component to the selected icon. The component name in this field must match the component name as it appears in the Component menu. The Browse button invokes the Find Component command to provide a simple way to assign the component to the icon. Finally, the All On, Default, and All Off buttons provide a quick way to set the display status for all of the icons in the main tool bar.

Adding a new component icon is an easy process. For this example, the independent current source, I, will be assigned to an icon and added to the main tool bar. First, select one of the blank icons. Next, create the design that will be used on the icon in the Draw Button area. For the current source, a simple source shape with an arrow in the middle of it was used to denote the component as seen in Figure 6. The third step is to assign the component name to the icon. The name 'I' can be typed directly into the field, or the Browse button can be used to find the component. Finally, enable either the checkbox next to the new icon or the Show Button checkbox. Modifying an existing component icon can be done in the same manner.

The new component tool bar appears in Figure 7 with the current source icon on the far right. The current source I is now available for one click selection for placement in the schematic.

Fig. 7 - Current Source Icon in the Component Tool Bar

Hysteresis Switch Macro

A hysteresis switch can be used in multiple applications such as oscillators or undervoltage-lockout systems. The switch primitives that are available in Micro-Cap 7 don't have hysteresis capabilities built into the models. In order to add this capability to one of the switches, a new macro circuit needs to be built using a switch primitive with added circuitry to handle the hysteresis. The macro and example circuits used in this article were derived based on a Christophe Basso article titled "Inline Equations Offer Hysteresis Switch in PSpice" that appears in the August 16, 2001 issue of EDN. The hysteresis switch macro circuit appears in Figure 8.

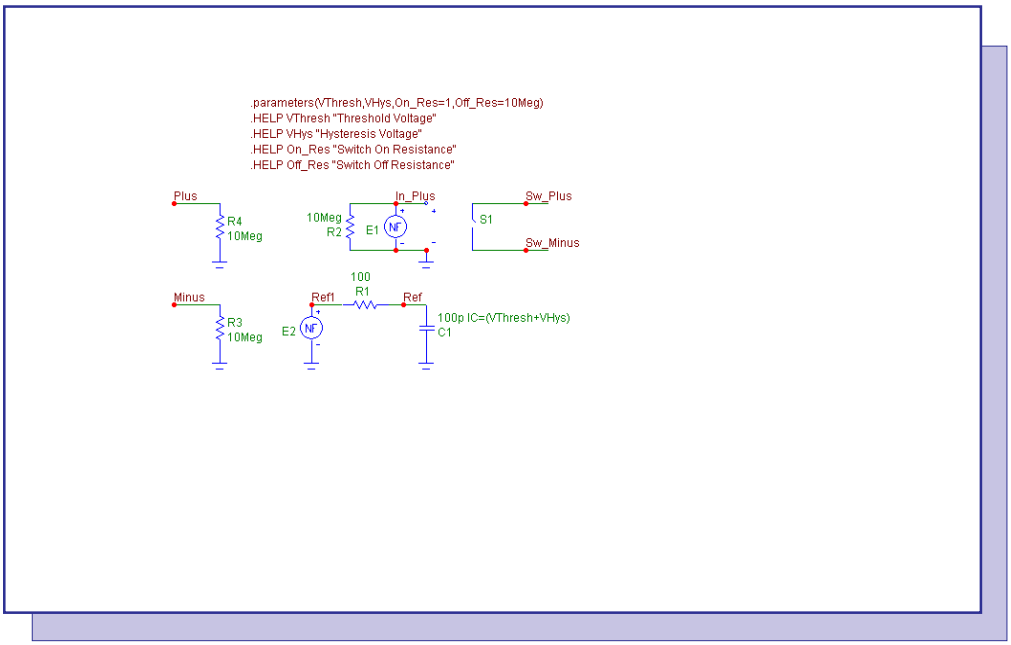


Fig. 8 - Hysteresis Switch Macro Circuit

The macro circuit has four input parameters: VThresh, VHys, On_Res, and Off_Res. The VThresh parameter defines the threshold voltage for the switch. The VHys parameter defines the hysteresis voltage that will be used with the threshold voltage to define the two toggling points. The high toggling point will be calculated as VThresh + VHys, and the low toggling point will be calculated as VThresh - VHys. The On_Res and Off_Res parameters define the on and off resistances for the switch.

The Plus and Minus nodes are the two voltage sensing input nodes for the macro. Each of these nodes has a 10Meg resistor going to ground to provide a high input resistance. The Sw_Plus and Sw_Minus nodes are the two output nodes of the macro and are on the outputs of a switch component. The switch, S1, in the macro is the S (V-Switch) component and is defined with the following model statement:

.MODEL SMOOTHSW VSWITCH (RON=On_Res ROFF=Off_Res VON=1 VOFF=0)

This voltage switch has a smooth transition when the voltage across its input nodes transitions between the VON and VOFF values. When the voltage is greater than VON, the resistance of the switch will be RON. When the voltage is less than VOFF, the resistance of the switch will be ROFF. In this case, a voltage of 1V or greater at the input will close the switch, and a voltage of 0V or less will open the switch. Between 0V and 1V, there is a smooth transition of the switch

resistance between its on and off states in order to aid in convergence. The two resistance values for the switch are defined by the On_Res and Off_Res parameters that are passed into the macro. The input nodes of the S1 switch sample the voltage of the E1 nonlinear function source. The E1 source has its VALUE attribute defined as:

If((V(Plus)-V(Minus)) > V(Ref), 1, 0)

The E1 source compares the differential voltage at the input nodes of the macro to the voltage at the node Ref in the macro circuit. If the input voltage is greater than the Ref voltage, the source produces a 1V output which closes the switch. When the input voltage is less than the Ref voltage, the source produces 0V which opens the switch.

The voltage at node Ref stores the toggling point of the switch. When the switch is open, the voltage at node Ref is equal to the high toggling point voltage, and when the switch is closed, the voltage at node Ref is equal to the low toggling point voltage. The difference between the two toggling points creates the hysteresis effect. The E2 nonlinear function source detects whether the switch is open or closed and produces the corresponding toggling point voltage. The VALUE attribute for the E2 source is defined as:

If(V(In_Plus) > .5, VThresh-VHys, VThresh+VHys)

If E2 detects that the voltage at node In_Plus is greater than .5V (closed switch), the source produces the low toggling point voltage (VThresh-VHys), and if the voltage at node In_Plus is less than .5V (open switch), the source produces the high toggling point voltage (VThresh+VHys). The resultant voltage is then stored at the Ref node on the C1 capacitor after a small RC time constant. The C1 capacitor has its initial condition arbitrarily set to the high toggling point.

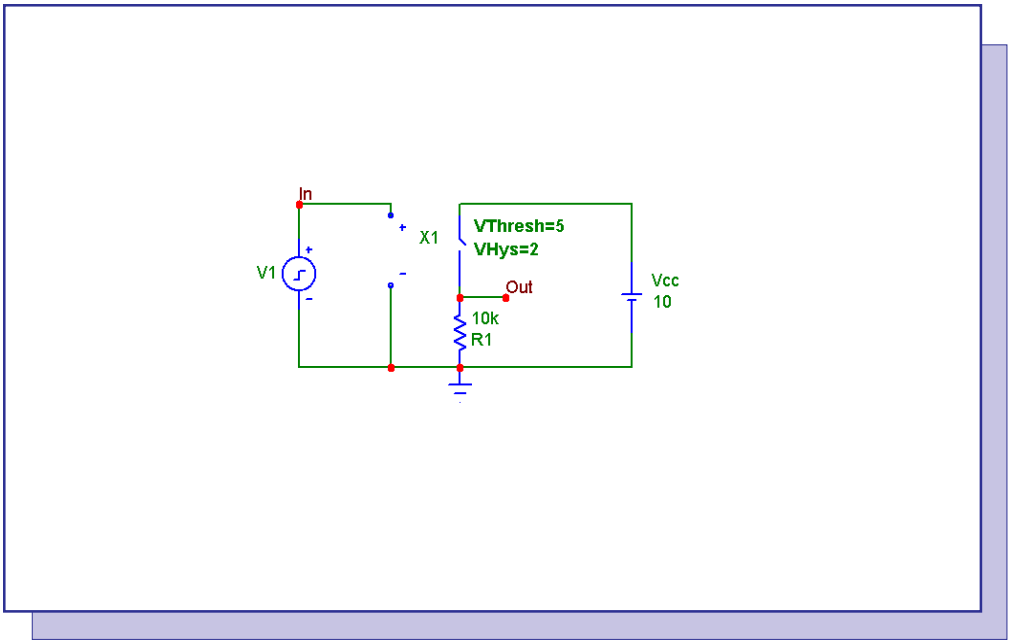


Fig. 9 - Hysteresis Switch Vout vs Vin Circuit

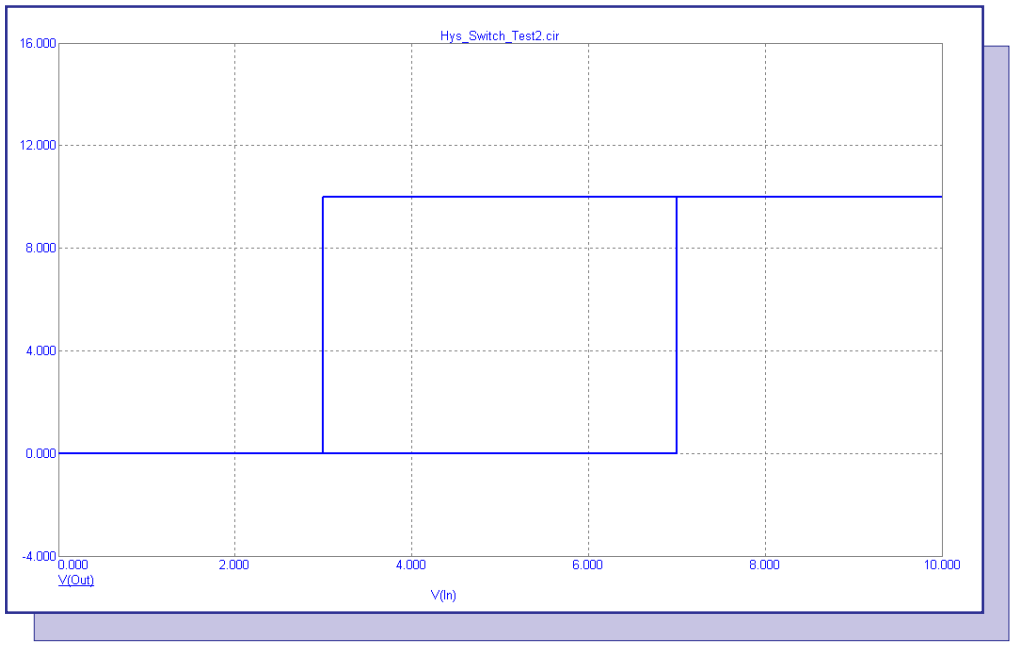


Fig. 10 - Hysteresis Switch Vout vs Vin Analysis

Two example circuits have been created to test the hysteresis switch macro. The first circuit appears in Figure 9. This circuit is designed to display the basic Vout vs Vin curve of the switch. The switch is placed in series between a battery and a resistor. The VThresh parameter is defined as 5V, and the VHys parameter is defined as 2V. The input of the switch is placed across a pulse source that creates a 10V, 2ms triangle wave. The transient analysis of this circuit appears in Figure 10. The analysis displays the traditional hysteresis waveform with the expected transition points at 3V and 7V, confirming the plus or minus 2V hysteresis.

The second circuit is a simple RC oscillator and appears in Figure 11. Again, the switch parameters have been set as VThresh=5V and VHys=2V. The transient analysis of the circuit appears in Figure 12. Note that the toggling points of the oscillator are at the expected 3V and 7V. In both of the example circuits, the on and off resistances of the switch were kept at the default values defined in the macro circuit .parameters statement.

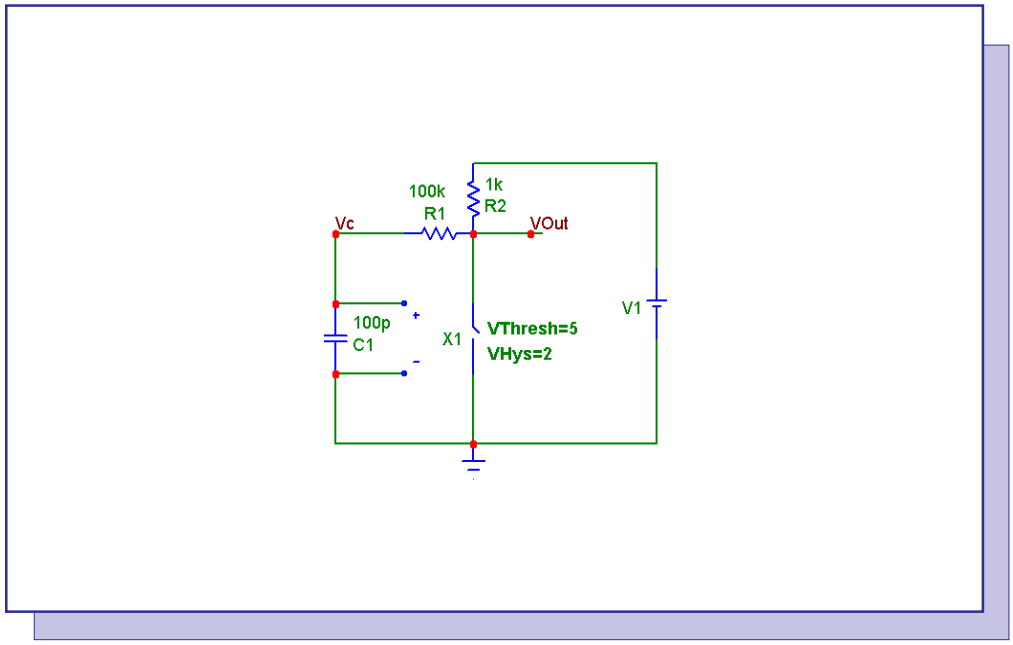


Fig. 11 - Oscillator Example Circuit

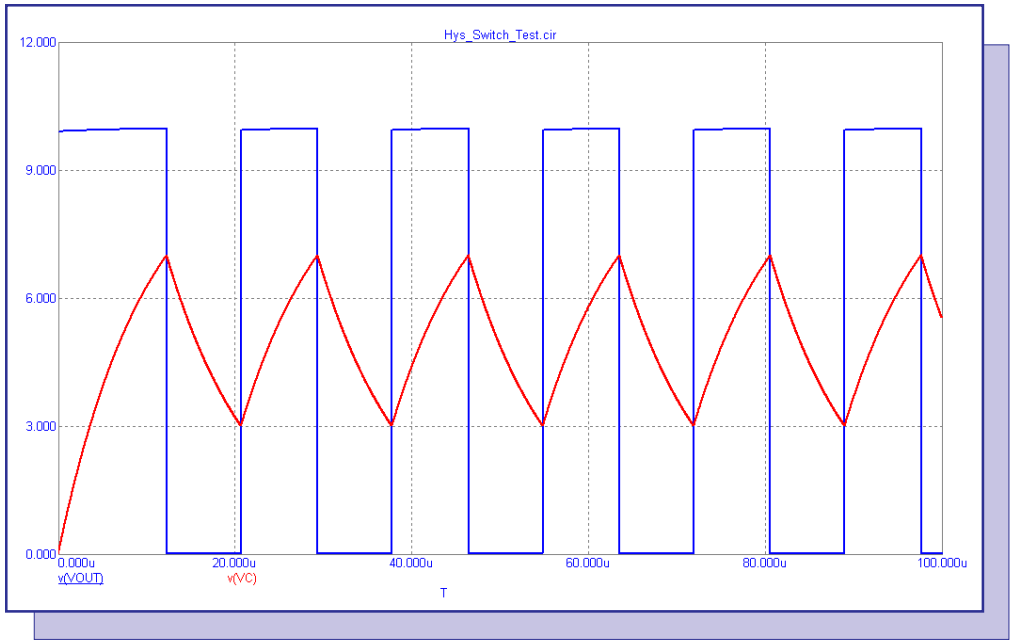


Fig. 12 - Oscillator Analysis

Product Sheet

Latest Version numbers

Micro-Cap 7 ..... Version 7.1.8
Micro-Cap 6 ..... Version 6.3.3
Micro-Cap V ..... Version 2.1.2

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