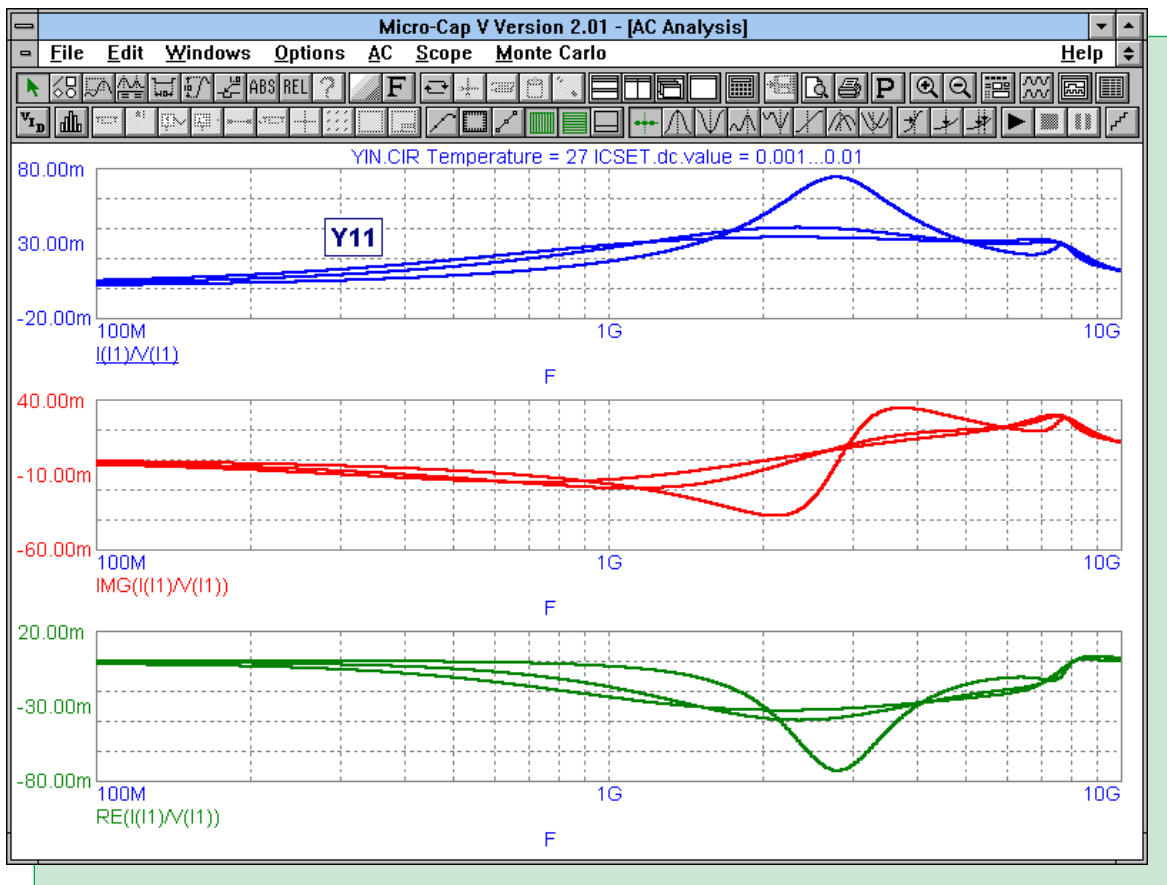


## Summer 1997

### Plotting Y Parameters



#### Featuring:

- Plotting Y Parameters
- Opamp Offset Parameters and Saturation
- Changing the Opamp Model for Different Power Supplies
- Using Performance Functions to Analyze a Filter

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## News In Preview

This issue features a couple of articles on the opamp model in Micro-Cap and what to beware of when using it. The two topics covered are the effect of the offset parameters in AC analysis, and how to adjust the opamp model when using different power supplies.

The newsletter also features an article on how to plot the Y parameters of a bipolar transistor, and how to use the new performance plot capability to analyze a filter.

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## Book Recommendations

- *Computer-Aided Circuit Analysis Using SPICE*, Walter Banzhaf, Prentice Hall 1989. ISBN# 0-13-162579-9
- *Macromodeling with SPICE*, Connelly and Choi, Prentice Hall 1992. ISBN# 0-13-544941-3
- *Semiconductor Device Modeling with SPICE*, Paolo Antognetti and Giuseppe Massobrio McGraw-Hill, Second Edition, 1993. ISBN# 0-07-002107-4
- *Inside SPICE-Overcoming the Obstacles of Circuit Simulation*, Ron Kielkowski, McGraw-Hill, First Edition, 1993. ISBN# 0-07-911525-X
- *The SPICE Book*, Andrei Vladimirescu, John Wiley & Sons, Inc., First Edition, 1994. ISBN# 0-471-60926-9
- *SMPS Simulation with SPICE 3*, Steven M. Sandler, McGraw Hill, First Edition, 1997. ISBN# 0-07-913227-8
- *MOSFET Modeling with SPICE Principles and Practice*, Daniel Foty, Prentice Hall, First Edition, 1997. ISBN# 0-13-227935-5

### German

- *Schaltungen erfolgreich simulieren mit Micro-Cap V*, Walter Gunther, Franzis', First Edition, 1997. ISBN# 3-7723-4662-6



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## Micro-Cap V Question and Answer

Caller: How do I step multiple resistors?

Tech: There are two methods to step multiple resistors. In the following two examples, two resistors will be stepped from 10k to 100k. These methods may be used for more than two resistors, or for capacitors and inductors.

### Using Model Statements

Place two resistors in the schematic with their attributes defined as follows:

PART	R1	R2
VALUE	10k	10k
MODEL	RDY	RDY

The RDY model statement should read: `.model RDY RES (R=1)`

This model statement can be edited in the text area of the schematic or through the Edit button in the Attribute dialog box, but the default model statement appears as above. Enter the appropriate analysis. Click on the Stepping command button in the Analysis Limits dialog box. In the Stepping dialog box, make sure that the Parameter Type is set to Model. The text fields in the Stepping dialog box should appear as:

Step What	RES RDY
	R
From	1
To	10
Step Value	1

The parameter R multiplies its value by the VALUE attribute of the resistors that reference it (10k in this case) to get the final resistance value. In this case, it will step the resistance from  $10k*1$  to  $10k*10$ .

### Using Symbolic Parameters

Place two resistors in the schematic with their attributes defined as follows:

PART	R1	R2
VALUE	RVAL	RVAL
MODEL		

In either the text area or the schematic itself, place the text `'.define RVAL 10k'`. Enter the appropriate analysis. Click on the Stepping command button in the Analysis Limits dialog box. In the Stepping dialog box, make sure that the Parameter Type is set to Symbolic. The text fields in the Stepping dialog box should appear as:

Step What	RVAL
From	10k
To	100k
Step Value	10k

This steps the symbolic parameter RVAL from 10k to 100k, and subsequently steps the two resistors that reference this parameter.

## Plotting Y Parameters

Y parameters or short-circuit admittance parameters are useful in the analysis of high frequency components. RF transistors, for example, are usually characterized by Y parameters. The following method extracts the Y parameters from a MRF9411 high frequency transistor from Motorola. This technique was derived from the article "Spice accepts and displays Y parameters" by Michael A. Wyatt which appears in the June 22, 1995 Design Ideas Supplement for EDN.

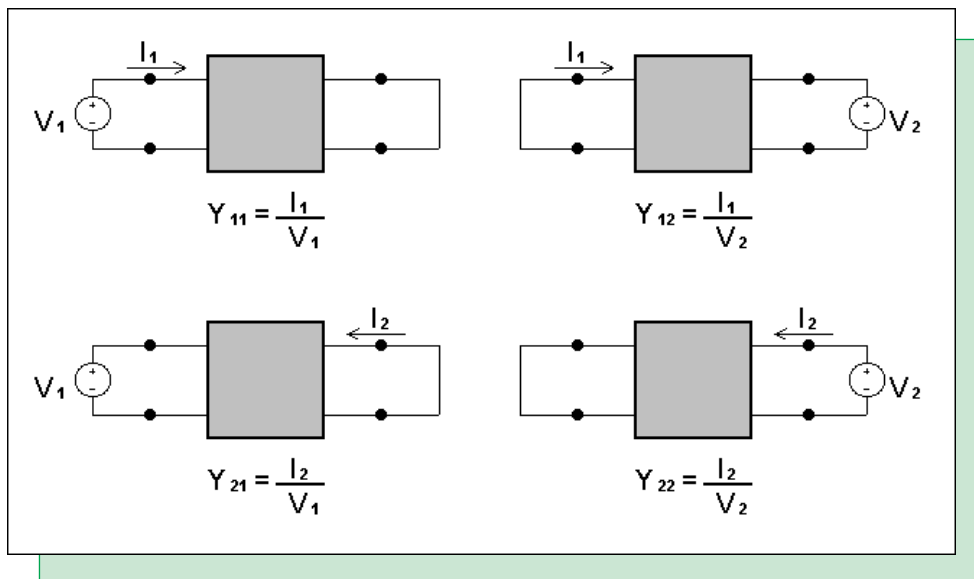
The Y parameters are based on exciting a two port network at one of its ports. The four admittance parameters are defined as follows.

$$\begin{aligned} I_1 &= Y_{11} V_1 + Y_{12} V_2 \\ I_2 &= Y_{21} V_1 + Y_{22} V_2 \end{aligned}$$

$$\begin{aligned} Y_{11} &= I_1 / V_1 \big|_{V_2=0} \\ Y_{12} &= I_1 / V_2 \big|_{V_1=0} \\ Y_{21} &= I_2 / V_1 \big|_{V_2=0} \\ Y_{22} &= I_2 / V_2 \big|_{V_1=0} \end{aligned}$$

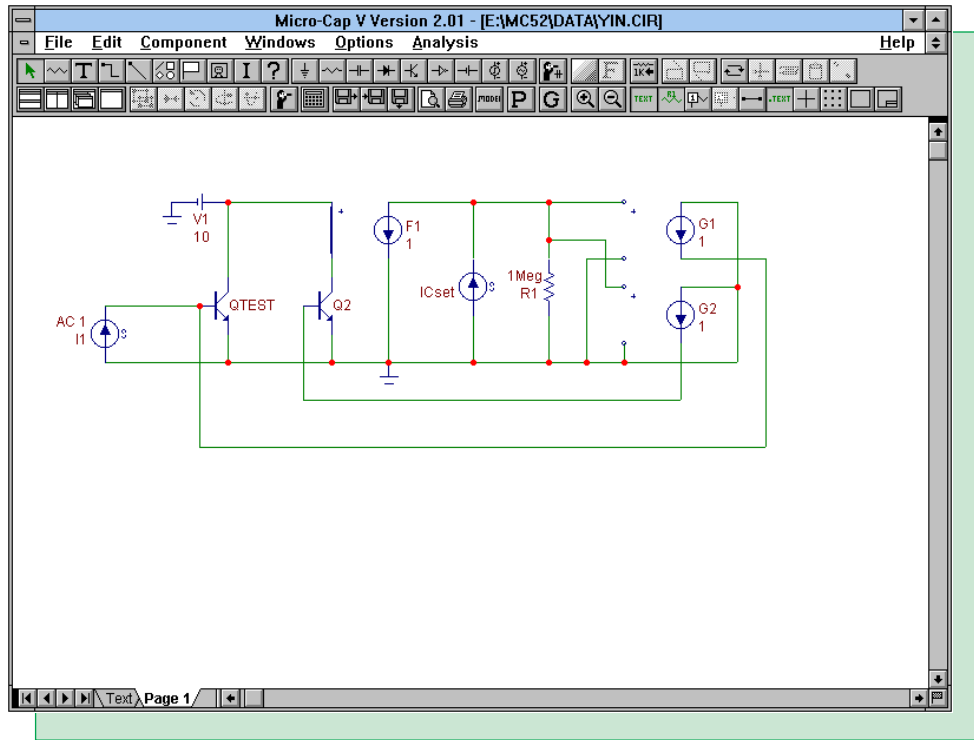
$Y_{11}$  is the input admittance at port 1 with port 2 short-circuited.  $Y_{12}$  represents the transmission from port 2 to port 1 with port 1 short-circuited.  $Y_{21}$  represents the transmission from port 1 to port 2 with port 2 short-circuited.  $Y_{22}$  is the admittance looking into port 2 with port 1 short-circuited.

The method for measuring each individual parameter would be to short one of the ports while exciting the other. Figure 1 displays the definition and method for measuring each of these parameters.



*Fig. 1 - Measurement circuits for Y parameters*

In order to plot the Y parameters versus frequency, an AC analysis needs to be run. The AC analysis is a small signal analysis. It initially calculates a DC operating point and then linearizes the devices about the operating point values. The trick to extracting Y parameters is to be able to bias the circuit correctly while still shorting one of the ports.



**Fig. 2 -  $Y_{11}$  and  $Y_{21}$  circuit**

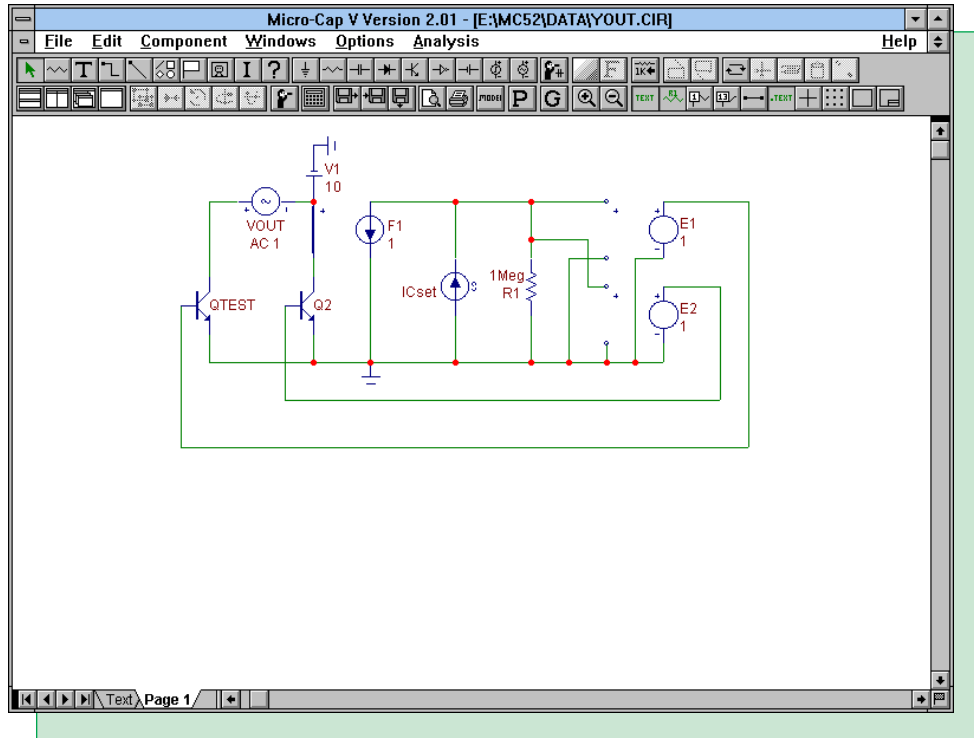
The circuit in Figure 2 will calculate the  $Y_{11}$  and  $Y_{21}$  parameters for the transistor QTEST, which is a MRF9411 high frequency transistor from Motorola. Q2 is also a MRF9411 transistor and is used to help bias QTEST.

V1, Q2, ICset, F1, R1, G1, and G2 are all used to bias QTEST during the DC operating point operation. The battery V1 supplies the DC supply voltage. During small signal analysis, the battery will act as a short circuit thus providing the circuit with the necessary short at port 2. Q2 is an image device which is identical to the QTEST transistor. ICset, F1, and R1 force the collector current for the two transistors to be equal to the current through ICset. ICset is defined as the value of the collector current that QTEST should be biased at. The current controlled current source, F1, samples the collector current of the Q2 transistor. The value of resistor R1 determines the accuracy of the collector current in relation to the ICset source. The larger the resistor, the closer the collector current will be to the ICset value. The collector current may be calculated through the following equation.

$$I_c = ICset / (1 + 1/(B * R1))$$

where B is the beta of the Q2 transistor. With a 1Meg R1 resistor, Ic and ICset are essentially equal. The voltage controlled current sources, G1 and G2, sample the voltage across R1 and produce a base current for each transistor. The base currents will be the same, which forces the collector currents in both transistors to be the same, so that QTEST has been biased with the current set by ICset.

During the small signal analysis, the F1, ICset, G1, and G2 current sources all act as open circuits so the DC bias point circuitry will have no effect. The only source that has been defined with an AC attribute is the current source I1. This source will provide a 1 Amp AC small signal source, exciting port 1, which in this case is the base of QTEST. Note that I1 has no DC component. This causes I1 to act as an open circuit during the DC bias point operation.



**Fig. 3 -  $Y_{12}$  and  $Y_{22}$  circuit**

The circuit in Figure 3 will extract the  $Y_{12}$  and  $Y_{22}$  parameters. This circuit operates in a similar manner to the previous circuit. V1, Q2, F1, ICset, and R1 again set the DC bias point for the QTEST transistor, and will have no effect during the small signal analysis. The voltage controlled voltage sources, E1 and E2, are used to bias the base of the transistors. Voltage sources were used in this case instead of the current sources of the previous circuit because the voltage sources will act as the necessary short circuit for port 1 during the small signal analysis. The only source with an AC attribute is the voltage source, Vout. This source provides a 1 Volt AC small signal source that excites port 2. Vout has no DC specification so that it will act as a short circuit during the DC bias point calculation.

Figures 4 through 7 display the results of these two circuits. Each of the figures displays one of the Y parameters along with its real and imaginary components. Note that in AC analysis, any complex value will automatically have its magnitude plotted, so the negative signs in the equations only have an effect when used in conjunction with the real and imaginary operators. In each of the runs, the ICset source has had its current stepped through the values of 1m, 5m, and 10m using the List option in the Stepping dialog box.

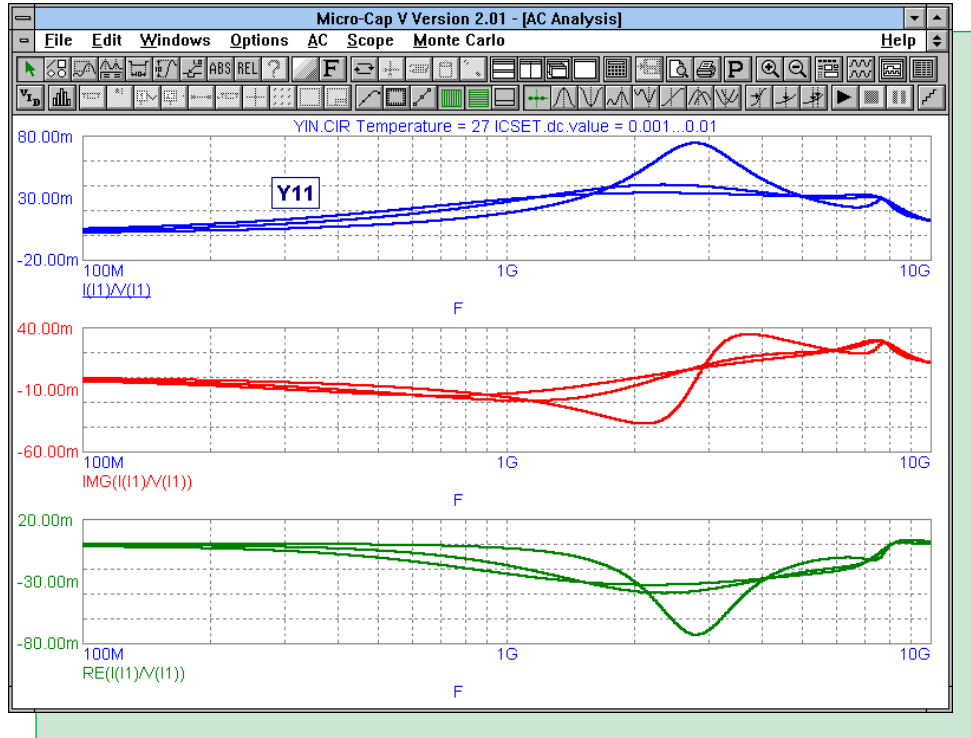


Fig. 4 -  $Y_{11}$  results

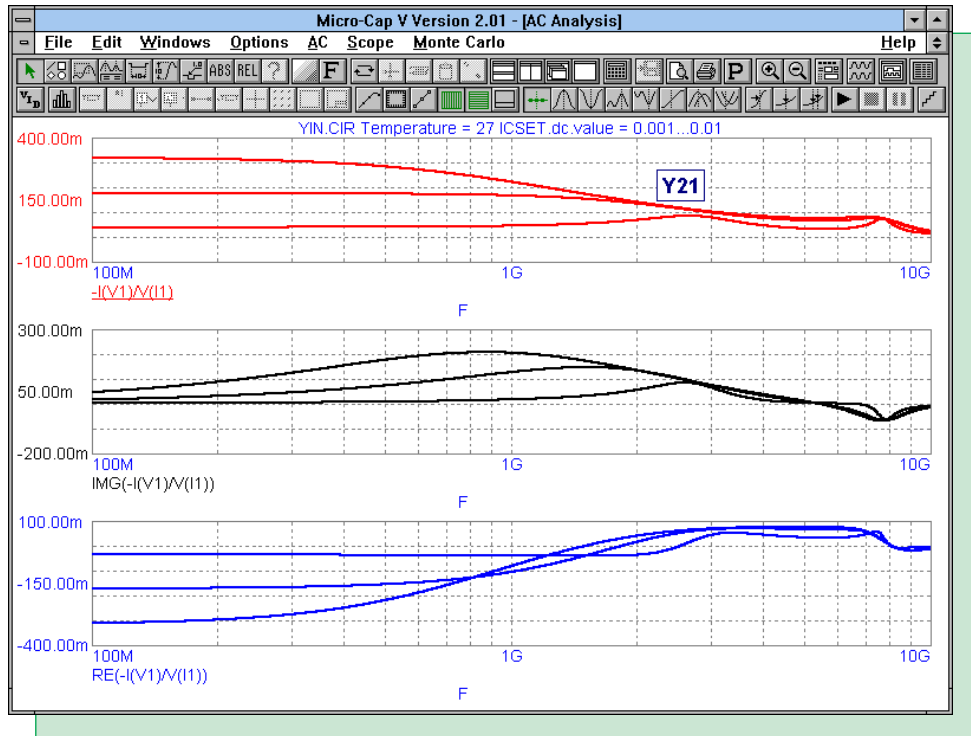


Fig. 5 -  $Y_{21}$  results



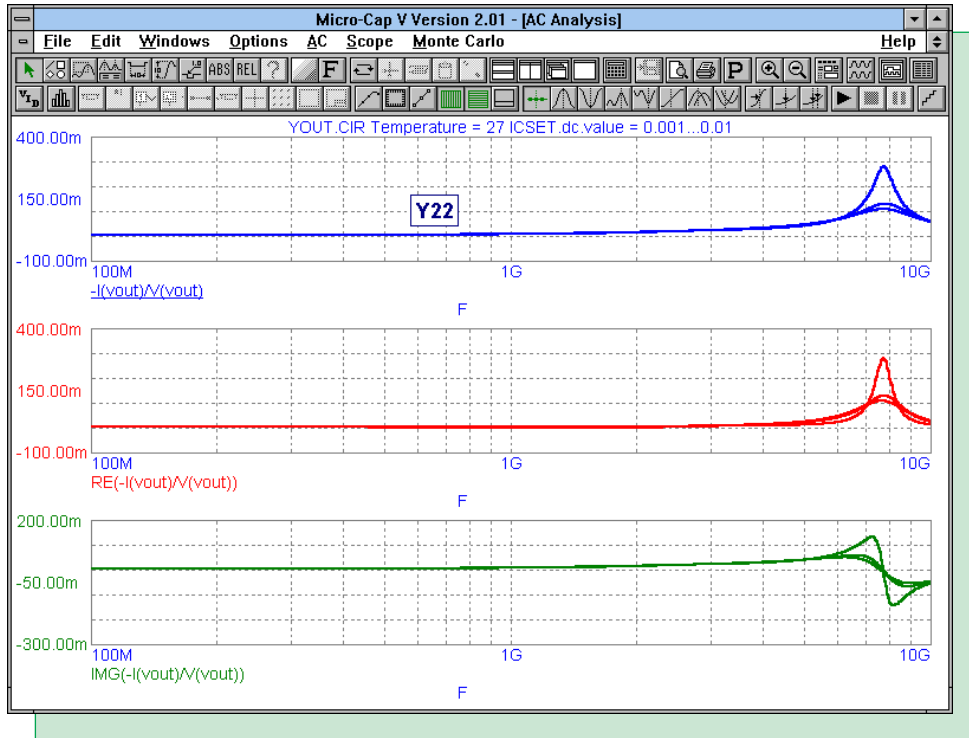


Fig. 6 -  $Y_{22}$  results

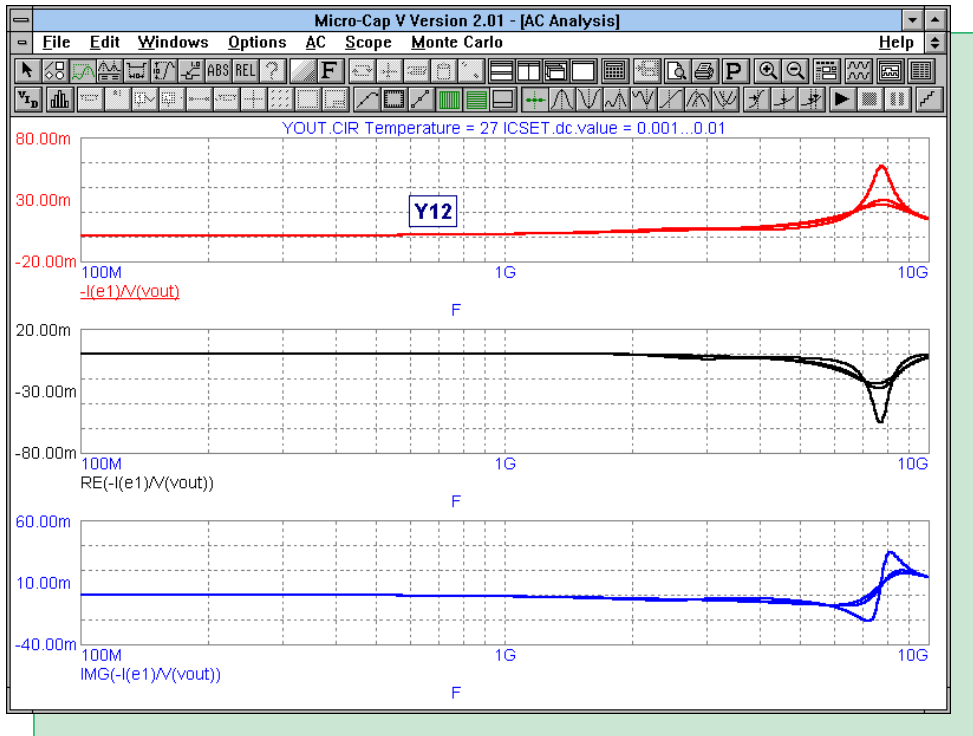
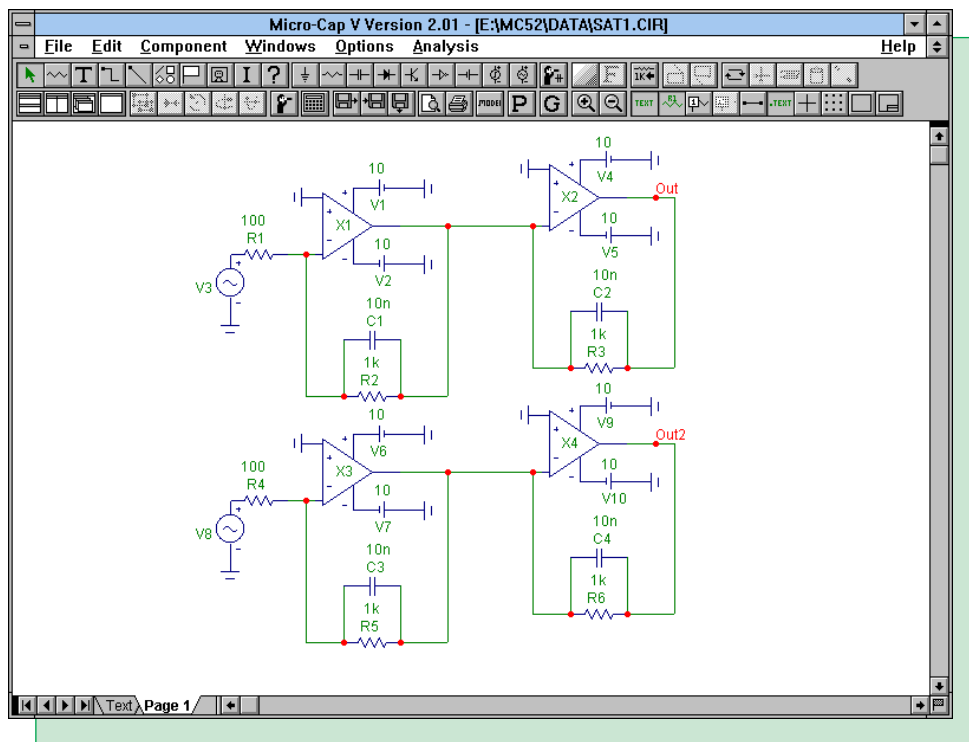


Fig. 7 -  $Y_{12}$  results

## Opamp Offset Parameters and Saturation

In AC analysis, a DC operating point is calculated at the beginning of the analysis. The circuit is then linearized around this calculated point. In simulating a circuit with an operational amplifier that uses a Micro-Cap .model statement, you have to be conscious of the effect that the three offset parameters may have on that DC operating point calculation. In high gain configurations, the offset parameters may wind up saturating the opamp at the operating point. The saturation would skew any expected results.

The three offset parameters are VOFF, IOFF, and IBIAS. VOFF is the input offset voltage. IOFF is the input offset current. IBIAS is the input bias current. In many data books, the offset parameters are only specified with their maximum values, so those would be the values specified in the library. Figure 8 displays a schematic that contains two identical circuits. Each of the circuits contains a pair of cascading opamps designed to produce a high gain. The top circuit uses the LF347 opamp model from the Micro-Cap library. The bottom circuit uses the LF347 model also, but the three offset parameters have been edited so they would not affect the simulation. VOFF has been set to 0, IOFF has been set to 0, and IBIAS has been set to 50f.



*Fig. 8 - Offset saturation schematic*

Figure 9 displays the DC operating point voltages for both circuits. The second opamp in the top circuit is saturated at -9.5 volts, while the second opamp in the bottom circuit is still in its linear area of operation at -6.8 volts. These are the voltages to which the circuit is to be linearized to. Since the top circuit is saturated, the full gain of the circuit will not be available for small signal analysis. This is apparent in Figure 10. The blue plots are for the top circuit, and the red plots are for the bottom circuit. Due to the offset saturation, the gain has dropped from 107dB to 14dB.

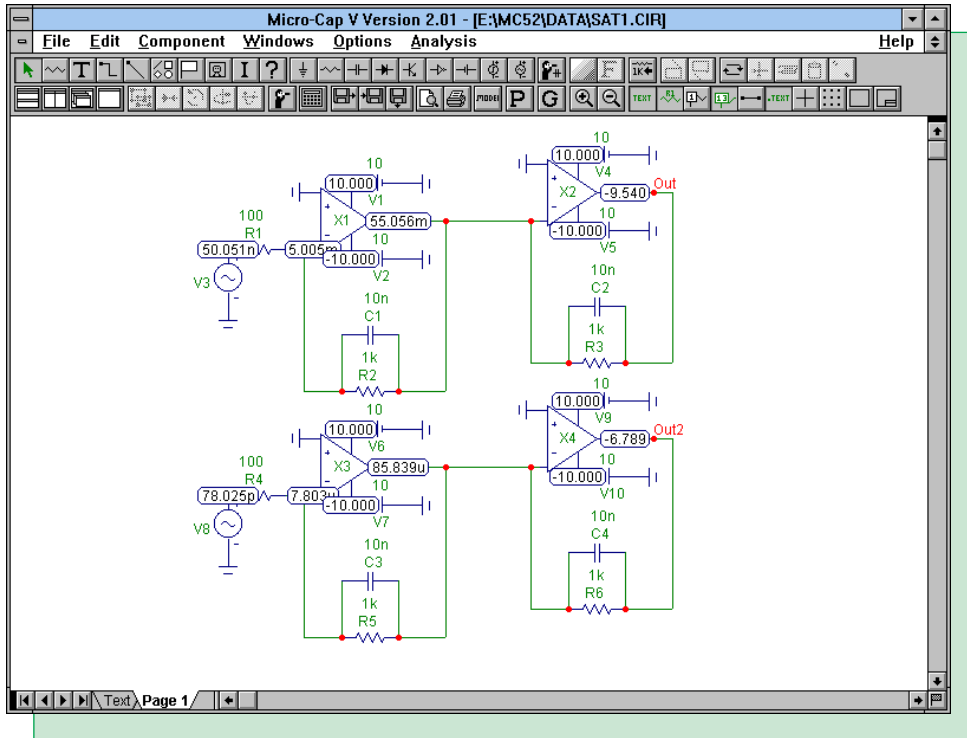


Fig. 9 - Operating point values

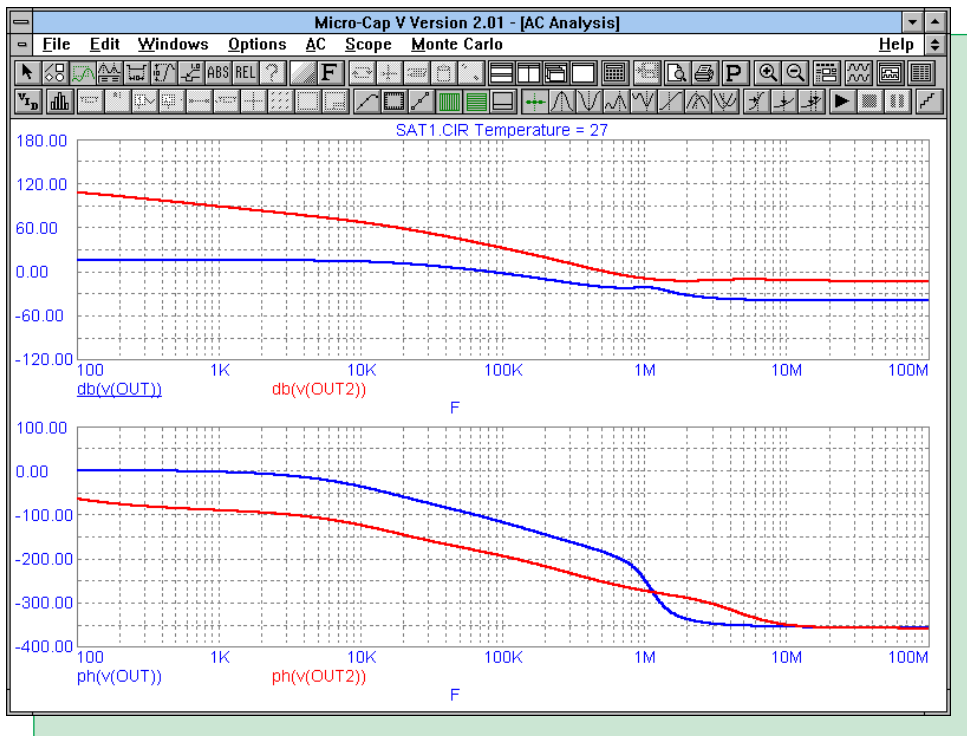


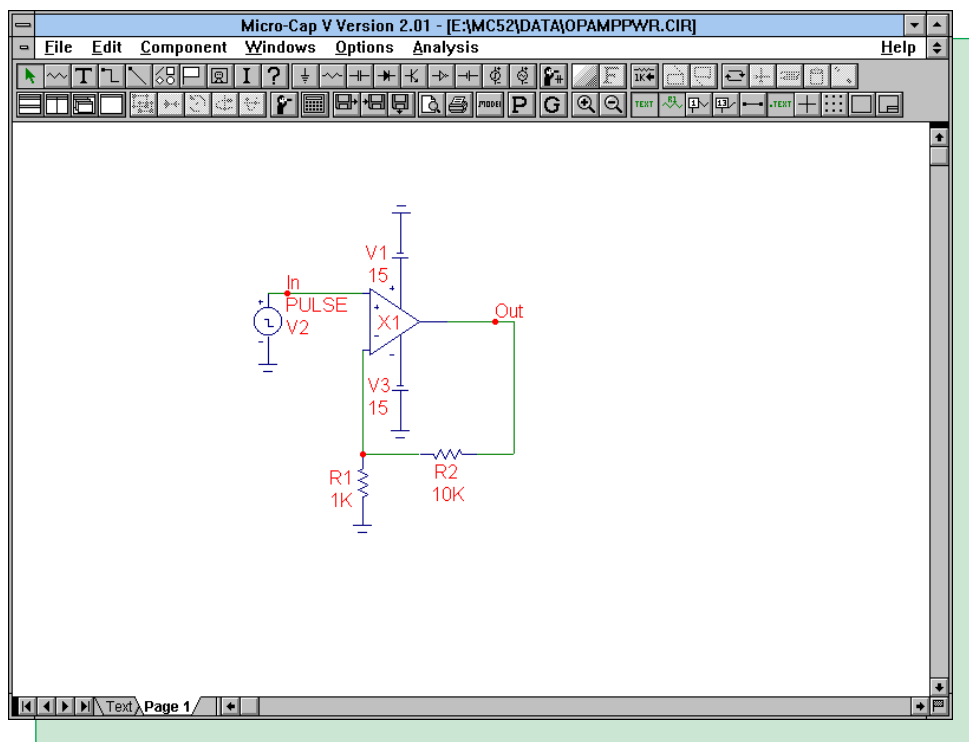
Fig. 10 - AC analysis results



## Changing the Opamp Model for Different Power Supplies

A typical opamp in circuit design today must be able to function at a variety of power supplies. Some must be able to operate on either a dual or a single rail. The opamp device model in Micro-Cap is capable of handling a wide range of power supplies. However, the opamp model can only have its output range set at one voltage. This means that if you would like to use anything but the standard power supply, usually  $\pm 15$  volts, the model may need to be edited.

There are four opamp parameters that control the point at which the opamp saturates: VCC, VEE, VPS, and VNS. VCC is the positive power supply. VEE is the negative power supply. VPS is the maximum positive voltage swing. VNS is the maximum negative voltage swing. The actual power supplies that the opamp uses are those that are connected to its power pins in the schematic. VCC and VEE only define the power supplies that the maximum voltage swings have been set at. Therefore, it is possible to have  $\pm 5$  volt power supplies on the schematic but have VCC and VEE set to  $\pm 15$  volts. To make the opamp run correctly with  $\pm 5$  volt power supplies, VCC, VEE, VPS, and VNS would all need to be changed.



*Fig. 11 - Opamp circuit with  $\pm 15$  volt power supplies*

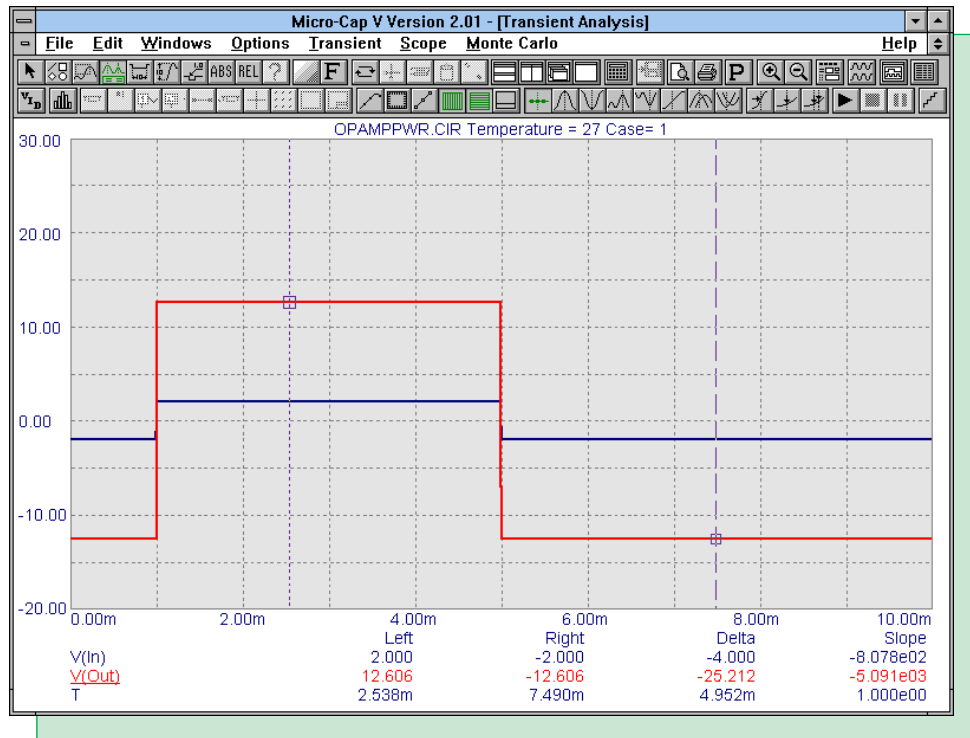
The circuit in Figure 11 has  $\pm 15$  volt power supplies in its schematic. The saturation parameters are: VCC=15, VEE=-15, VPS=12, and VNS=-12. What these parameters actually do is determine an offset from the power supply that the opamp will saturate at. It calculates the offset through the following equations:

Positive saturation = VCC - VPS - diode drop

Negative saturation = -VEE + VNS - diode drop

For the circuit above, the positive saturation offset and negative saturation offset will both be approximately 2.4.

The analysis of the circuit appears in Figure 12. A pulse going from -2 volts to 2 volts is input to ensure saturation. As can be seen below, the output of the opamp has saturated at  $\pm 12.606$  volts which corresponds to the offsets of 2.4 volts.



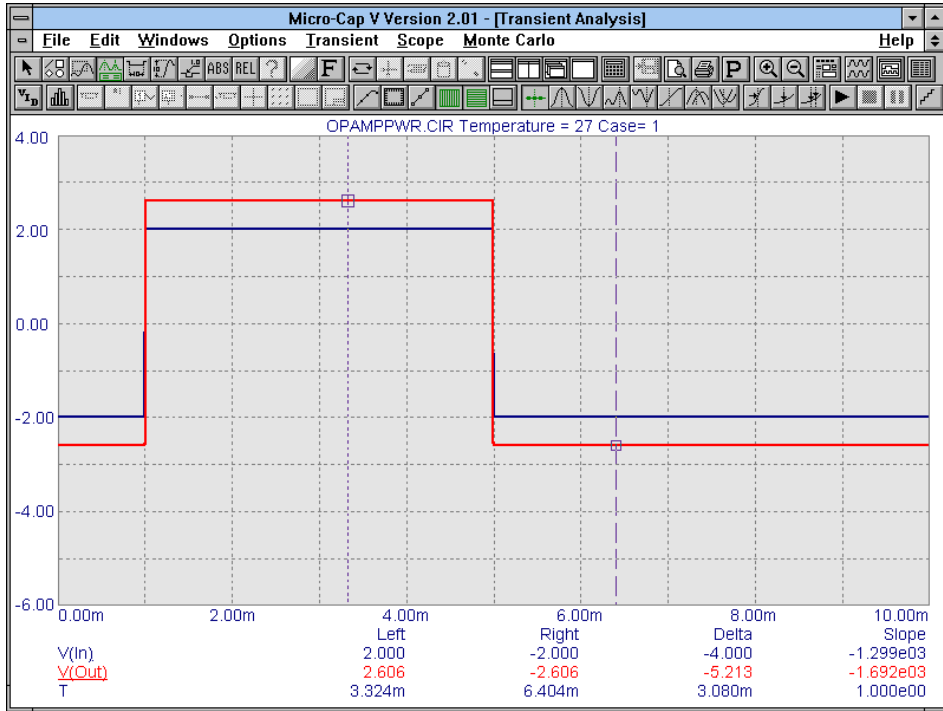
**Fig. 12 - Analysis with  $\pm 15$  volt power supplies**

The power supplies on the circuit are now changed to  $\pm 5$  volts. Figure 13 displays the analysis of this circuit. The opamp now saturates at 2.606 and -2.606. A real opamp with  $\pm 5$  volt power supplies would probably saturate at about  $\pm 4$  volts. The problem here is that the opamp is still using the 2.4 volt offsets calculated before and now applying it to the  $\pm 5$  volt power supplies.

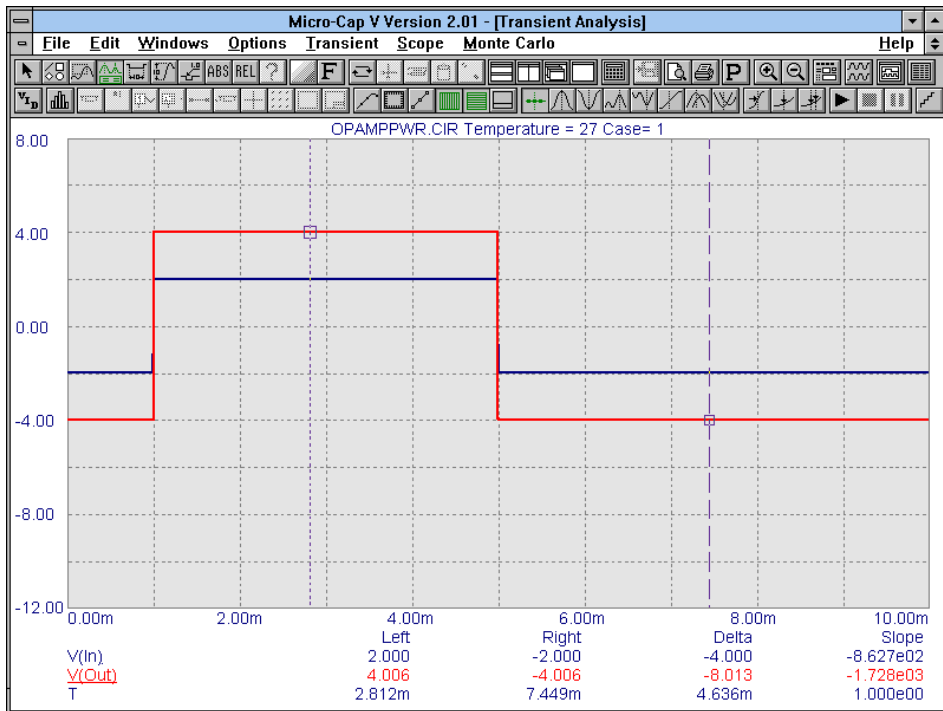
To make the opamp work correctly, the saturation parameters need to be edited. Assuming that we want the opamp to saturate at  $\pm 4$  volts, the parameters are changed as follows:

VCC=5  
 VEE=-5  
 VPS=3.4  
 VNS=-3.4

These values produce the desired 1 volt offset. Figure 14 displays the analysis with the edited parameters. The range of the opamp now goes from 4.006 to -4.006. In order to use the opamp model efficiently, these four parameters always need to be checked versus the power supply that is going to be used on the schematic.



*Fig. 13 - Analysis with  $\pm 5$  volt power supplies*

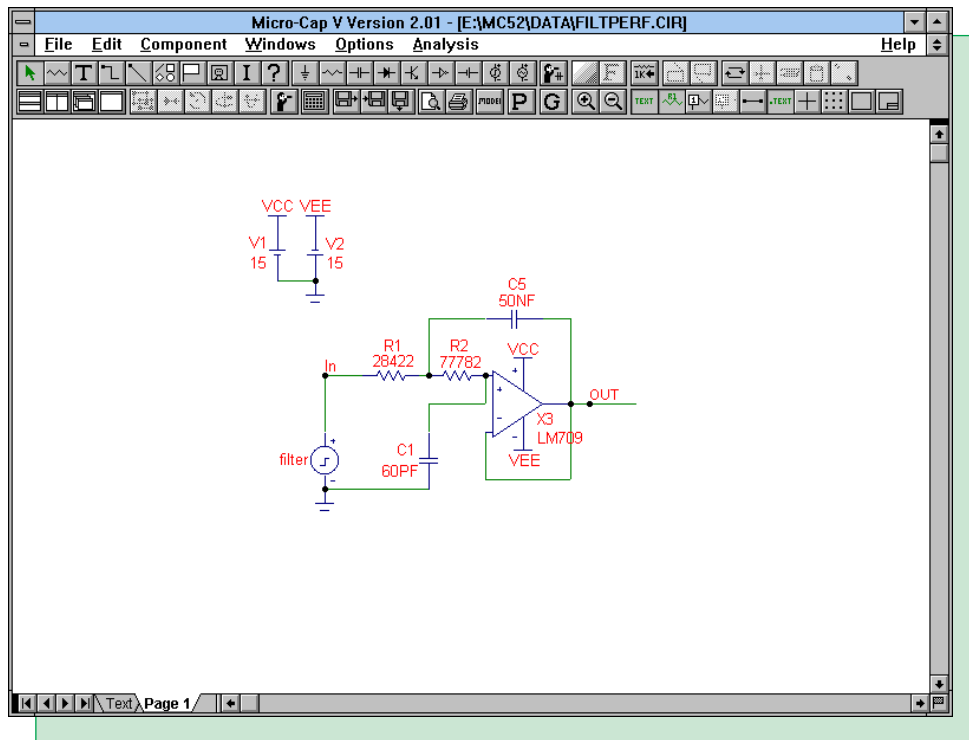


*Fig. 14 - Analysis with  $\pm 5$  volt power supplies and edited parameters*

## Using Performance Functions to Analyze a Filter

Performance functions are mathematical procedures designed to aid in extracting measures of circuit performance from waveforms generated during an analysis. Micro-Cap provides functions to measure performance related values such as rise time, width, peak, valley, high, low, and many others. A useful feature of the performance functions is in creating performance plots. Performance plots may only be used when at least one parameter, including temperature, in the circuit is being stepped. A performance plot is created by plotting one data point from each stepped run that matches the criteria of a specified performance function.

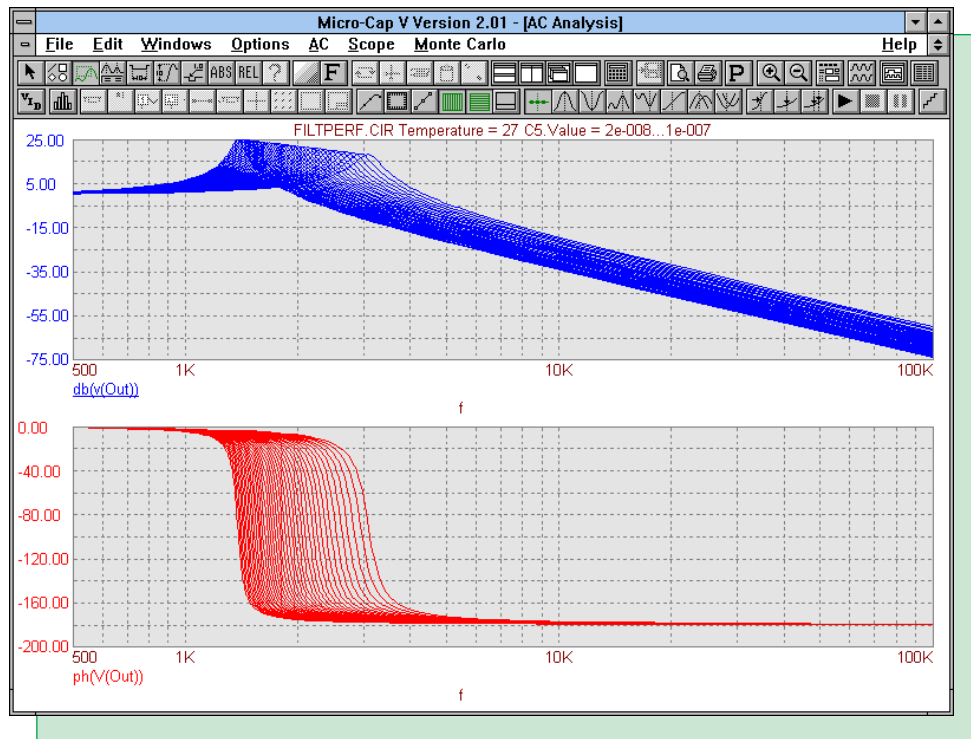
Performance functions are useful for any type of circuit. In the example that follows, a couple of performance functions will be used to aid in the analysis of a filter.



*Fig. 15 - Active Chebyshev filter*

The circuit in Figure 15 is an active Chebyshev filter. This circuit is modified from one available in the FILTER.CIR file. The pulse source 'Filter' provides an AC small signal source of 1 volt magnitude. The opamp LM709 is actually an ideal level 1 opamp model that only models the gain and finite output resistance.

Figure 16 displays the AC analysis of the gain and phase waveforms at node 'Out'. The feedback capacitor, C5, has been stepped from 20nF to 100nF in steps of 2nF. For increasing values of the feedback capacitor, the bandwidth gets smaller and the ripple gets larger. The bandwidth and the ripple are the two waveform characteristics that will be analyzed through the use of performance plots.



**Fig. 16 - AC analysis of gain and phase**

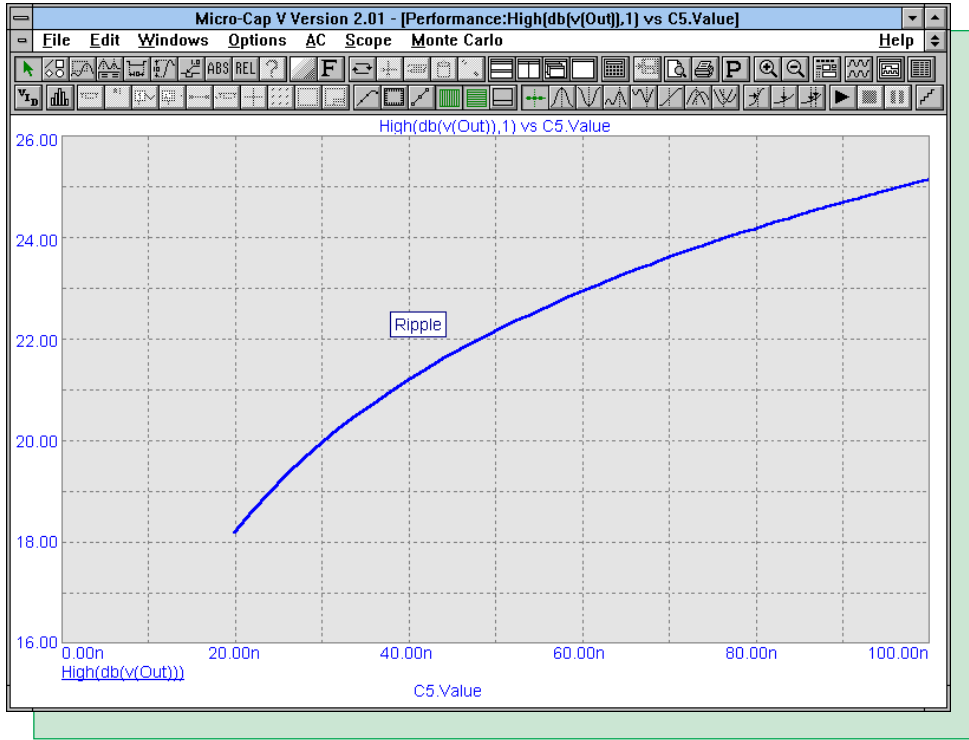
To plot the performance plot of the ripple versus the stepped capacitor, we will use the performance function High on the dB(V(Out)) waveform. The High function finds the global maximum of each stepped run, and then returns the maximum of each run for plotting. Figure 17 displays the performance plot of the ripple versus the capacitance of C5. The plot shows the ripple increasing as the capacitor is increased which is as expected. The performance function Peak may also have been used in this case, but since the ripple is the highest data point in the plot, High is easier to use.

To plot the performance plot of the bandwidth versus the stepped capacitor, we will use the performance function X\_Level on the dB(V(Out)) waveform. The X\_Level performance function has two parameters, N and Y Level. This function will find the Nth instance of the specified Y Level value, and it will then return the corresponding X value for that expression. In this case, N is specified as 1, and Y Level is specified as -3. Therefore, the first time that the function finds the -3dB level of the gain waveform, it will return the corresponding frequency at which this occurs. This will give us the bandwidth value. Figure 18 displays the performance plot of the bandwidth versus the capacitance of C5. As expected, the bandwidth decreases when the capacitor is increased.

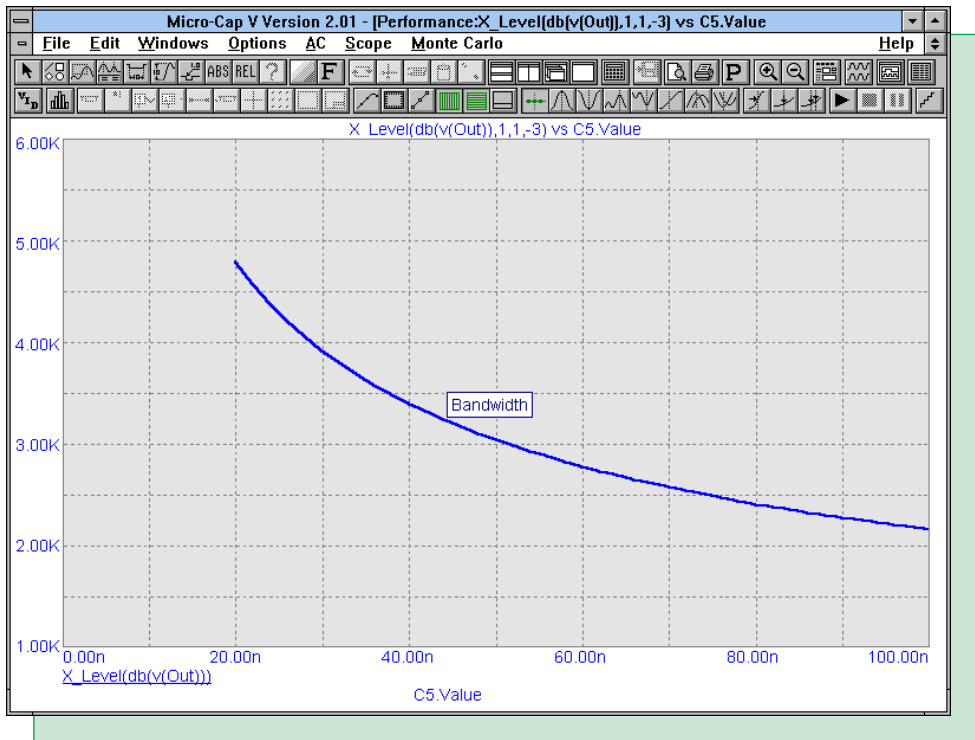
Performance functions may be used on any waveform that is plotted. In the above examples, we could have also used the ph(V(Out)) waveform if that would have provided us with the appropriate information.

In addition to performance plots, another way to view data from stepped waveforms is through 3D plots. This can be a powerful way to visualize the simulation results from a stepping operation. Figure 19 is a 3D plot of the gain vs frequency vs the capacitance of C5. However, the default patch size of 40 X 40 does not adequately sample the ripple of the filter for many of the steps.

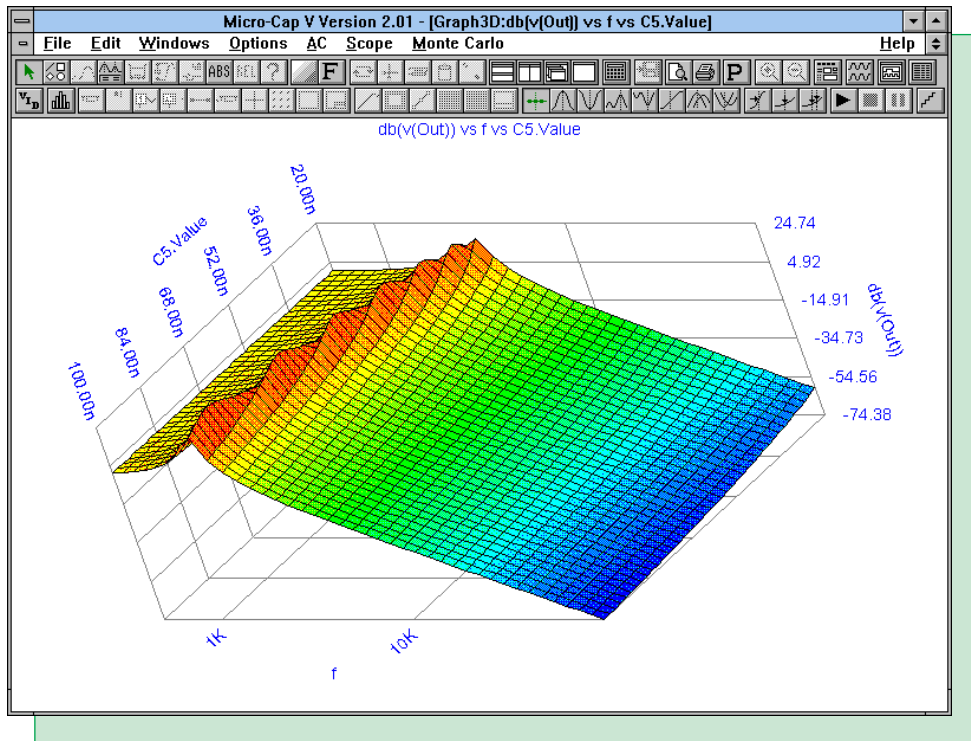




**Fig. 17 - Performance plot of ripple versus capacitance of C5**

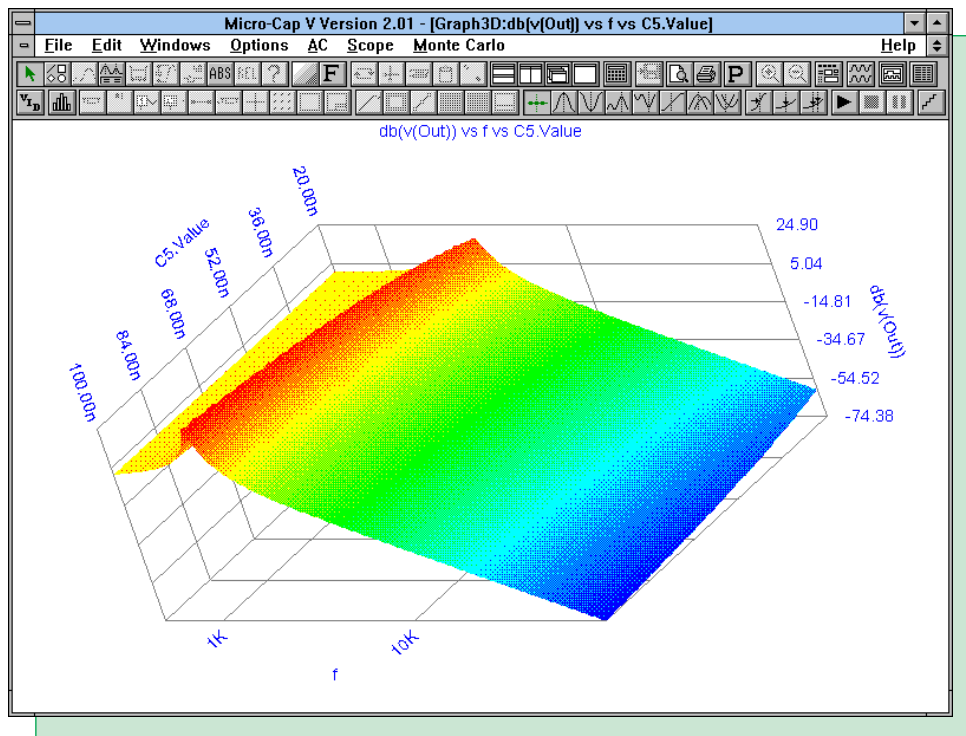


**Fig. 18 - Performance plot of bandwidth versus capacitance of C5**



**Fig. 19 - 3D plot of  $db(V(Out))$  vs  $F$  vs capacitance of  $C5$**

To sample the ripple precisely, the patches of the 3D plot need to be increased to 200 X 200. This measures the ripple correctly, but the isolines then need to be turned off because they become too close together and cover the plot. Figure 20 displays the same 3D plot with increased resolution and with its isolines disabled.



**Fig. 20 - 3D plot with increased resolution**

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## Product Sheet

### Latest Version numbers

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Micro-Cap IV IBM/NEC/MAC ..... Version 3.04

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