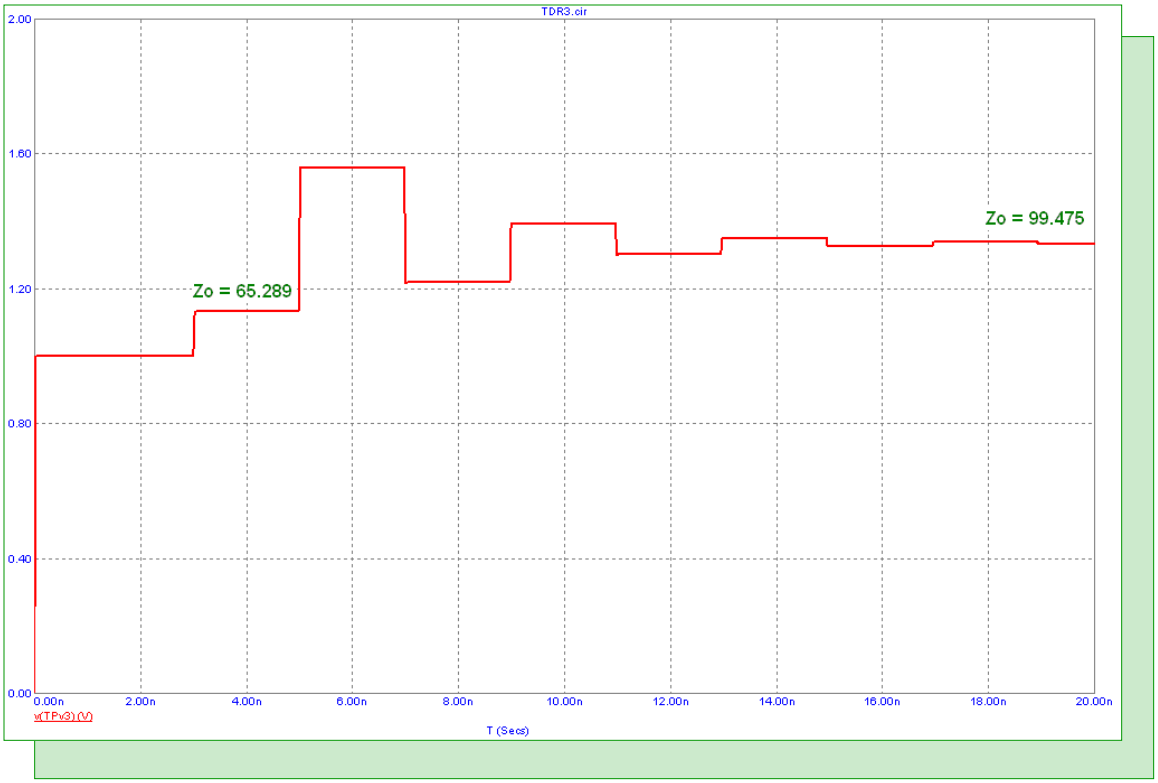
Spectrum News

Applications for Micro-Cap™ Users

Summer 2011

News



Simulating TDR Measurements

Featuring:

- Diode If vs Vf Temperature Modeling
- Simulating TDR Measurements
- Measuring Power Factor in Linear Circuits

News In Preview

This newsletter's Q and A section describes how to couple inductors together either linearly or with the nonlinear Jiles-Atherton magnetics model. The Easily Overlooked Feature section describes the pop up menus available when the mouse is right clicked in the Page or P fields within the Analysis Limits dialog box. These menus provide a quick way to sort, enable, hide, or disable groups of waveforms.

The first article describes how to optimize the XTI, TRS1, and TRS2 model parameters for the diode to produce accurate forward voltage versus forward current curves with respect to temperature.

The second article describes time domain reflectometry (TDR) which is a method by which a short duration pulse with a very fast rise time is injected into an electrical line. The reflected waveform from this pulse can be used to calculate the characteristics of the line such as the impedances and propagation delays along the signal path.

The third article describes how to use performance functions to measure the power factor in a linear circuit.

Contents

Book Recommendations

General SPICE

• *Computer-Aided Circuit Analysis Using SPICE*, Walter Banzhaf, Prentice Hall 1989. ISBN# 0-13-162579-9

• *Macromodeling with SPICE*, Connelly and Choi, Prentice Hall 1992. ISBN# 0-13-544941-3

• *Inside SPICE-Overcoming the Obstacles of Circuit Simulation*, Ron Kielkowski, McGraw-Hill, 1993. ISBN# 0-07-911525-X

• *The SPICE Book,* Andrei Vladimirescu, John Wiley & Sons, Inc., 1994. ISBN# 0-471-60926-9

MOSFET Modeling

• *MOSFET Models for SPICE Simulation, William Liu, Including BSIM3v3 and BSIM4*, Wiley-Interscience, ISBN# 0-471-39697-4

Signal Integrity

• *Signal Integrity and Radiated Emission of High-Speed Digital Signals*, Spartaco Caniggia, Francescaromana Maradei, A John Wiley and Sons, Ltd, First Edition, 2008 ISBN# 978-0-470-51166-4

Micro-Cap - Czech

• *Resime Elektronicke Obvody,* Dalibor Biolek, BEN, First Edition, 2004. ISBN# 80-7300-125-X

Micro-Cap - German

• *Simulation elektronischer Schaltungen mit MICRO-CAP,* Joachim Vester, Verlag Vieweg+Teubner, First Edition, 2010. ISBN# 978-3-8348-0402-0

Micro-Cap - Finnish

• *Elektroniikkasimulaattori,* Timo Haiko, Werner Soderstrom Osakeyhtio, 2002. ISBN# 951-0-25672-2

Design

• *High Performance Audio Power Amplifiers,* Ben Duncan, Newnes, 1996. ISBN# 0-7506-2629-1

• *Microelectronic Circuits,* Adel Sedra, Kenneth Smith, Fourth Edition, Oxford, 1998

High Power Electronics

• *Power Electronics,* Mohan, Undeland, Robbins, Second Edition, 1995. ISBN# 0-471-58408-8

• *Modern Power Electronics,* Trzynadlowski, 1998. ISBN# 0-471-15303-6

Switched-Mode Power Supply Simulation

• *SMPS Simulation with SPICE 3,* Steven M. Sandler, McGraw Hill, 1997. ISBN# 0-07-913227-8

• *Switch-Mode Power Supplies Spice Simulations and Practical Designs*, Christophe Basso, McGraw-Hill 2008. This book describes many of the SMPS models supplied with Micro-Cap.

Micro-Cap Questions and Answers

Question: I would like to simulate coupling between multiple inductances in my circuit. I have placed the inductor components in the correct locations. How do I couple these inductors together?

Answer: The K component available in Micro-Cap will couple inductors using either the linear mutual inductance or the nonlinear Jiles-Atherton core magnetics model. The K component is located in the Analog Primitives / Passive Components section of the Component menu. The procedure for each of the possible couplings is as follows:

Linear Mutual Inductance
1) Place an inductor component in the schematic for each inductance that is to be coupled. The INDUCTANCE attribute of each inductor should be defined with the corresponding inductance value.

2) Place a K component in the schematic. The K component has no external connections so it can be placed anywhere in the circuit. The INDUCTORS attribute needs to be defined with the part name of each inductor that is to be coupled. For example, if the inductors L1, L4, and L6 were to be coupled together, the INDUCTORS attribute should be specified as:

L1 L4 L6

A minimum of two inductors must be in this list. The COUPLING attribute should then be defined with the coupling coefficient value. The MODEL attribute needs to remain undefined.

Upon hitting OK in the Attribute dialog box, the specified inductors will then be coupled.

Nonlinear Jiles-Atherton core magnetics model
1) Place an inductor component in the schematic for each winding that is to be coupled. The INDUCTANCE attribute of each inductor should be defined with the number of turns for the winding. The number of turns must be a constant, whole number.

2) Place a K component in the schematic. The INDUCTORS and COUPLING attributes need to be defined in the same manner as the above procedure. In this case, the list can contain just one inductor. A single inductor will create a single magnetic core device not coupled to another inductor. The MODEL attribute must then be defined with the name of a core model. The presence of a model name signifies that this coupling will use the Jiles-Atherton model.

Upon hitting OK in the Attribute dialog box, the specified inductors will now use the nonlinear Jiles-Atherton magnetics model.

Easily Overlooked Features

This section is designed to highlight one or two features per issue that may be overlooked among all the capabilities of Micro-Cap.

Page and P field Pop Up Menus in the Analysis Limits dialog box
The Page and P fields within the Analysis Limits dialog box specify the location of the corresponding waveform. The Page field specifies which analysis page the waveform will be displayed in, and the P field specifies which plot group the waveform will be displayed in.

Right clicking in any of the Page or P fields invokes a pop up menu that provides the following operations:

Sort - For the Page field, this sorts all of the expressions in the analysis limits so that the page names are in alphabetical order. For the P field, this sorts all of the expression in the analysis limits by the value in the P column.

Enable - For the Page field, all expressions that share the same page name will have their status set to enabled. For the P field, all expressions that share the same P value and the same page name will have their status set to enabled.

Hide - For the Page field, all expressions that share the same page name will have their status set to hidden. For the P field, all expressions that share the same P value and the same page name will have their status set to hidden. A hidden waveform is one whose data is stored in memory during the simulation, but the waveform is not initially displayed in the plot. The waveform can be added to a plot after the simulation is finished within the Plot page of the Properties dialog box.

Disable - For the Page field, all expressions that share the same page name will have their status set to disabled. For the P field, all expressions that share the same P value and the same page name will have their status set to disabled.

For the enabled and hidden waveforms, a valid value in the P column must also be specified for these waveforms to be calculated. If the P column is blank, the waveform is disabled no matter what the status is set to.

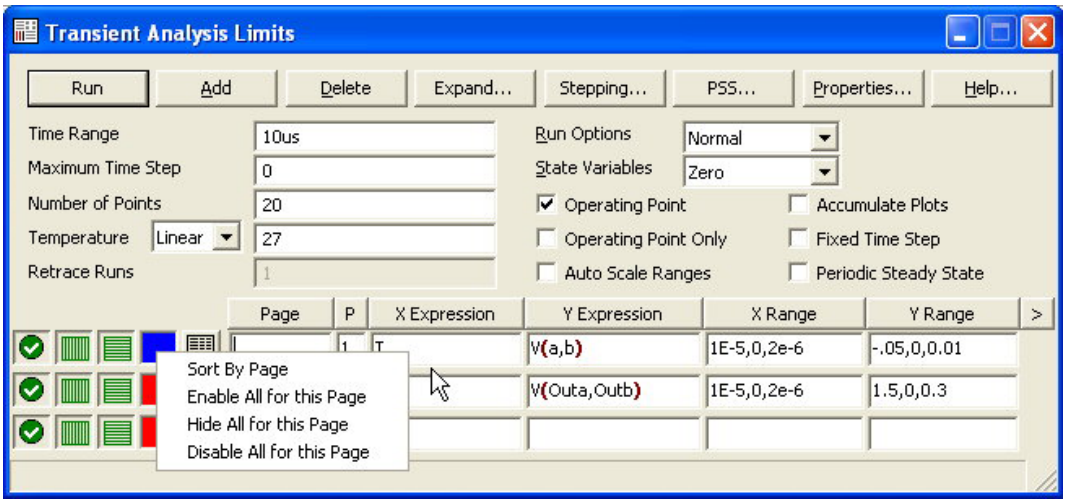


Fig. 1 - Page field right click menu

Diode If vs Vf Temperature Modeling

For many SPICE models, temperature modeling has not been optimized. The temperature parameters that affect the characteristic curves of the model are typically left at their default values which may not be accurate for simulations whose temperature setting deviates from the temperature that the model's parameters were optimized at. Most device models are optimized at either 25 or 27 degrees Celsius which is considered room temperature. The circuit optimizer that is available in transient, AC, or DC analysis for Micro-Cap can be used to derive the temperature parameter values for more accurate simulation results.

For the basic forward current versus forward voltage curve of a diode, the three primary temperature parameters in the diode model are XTI, TRS1, and TRS2. XTI is the saturation current temperature coefficient and is used to change the diode saturation current sensitivity. The TRS1 and TRS2 parameters are the temperature coefficients for the series resistance in the diode model. The TRS1 is the linear coefficient, and the TRS2 is the quadratic coefficient. These two parameters operate in the same manner as the temperature coefficients for the resistor component.

The circuit below is used to plot the forward current versus forward voltage curve. The diode model is the 1N3879 fast recovery power rectifier whose data was derived from the Motorola "Rectifiers and Zener Diodes" data book. The only other component in the schematic is a battery with the part name Vf that will be used to sweep the forward voltage across the diode.

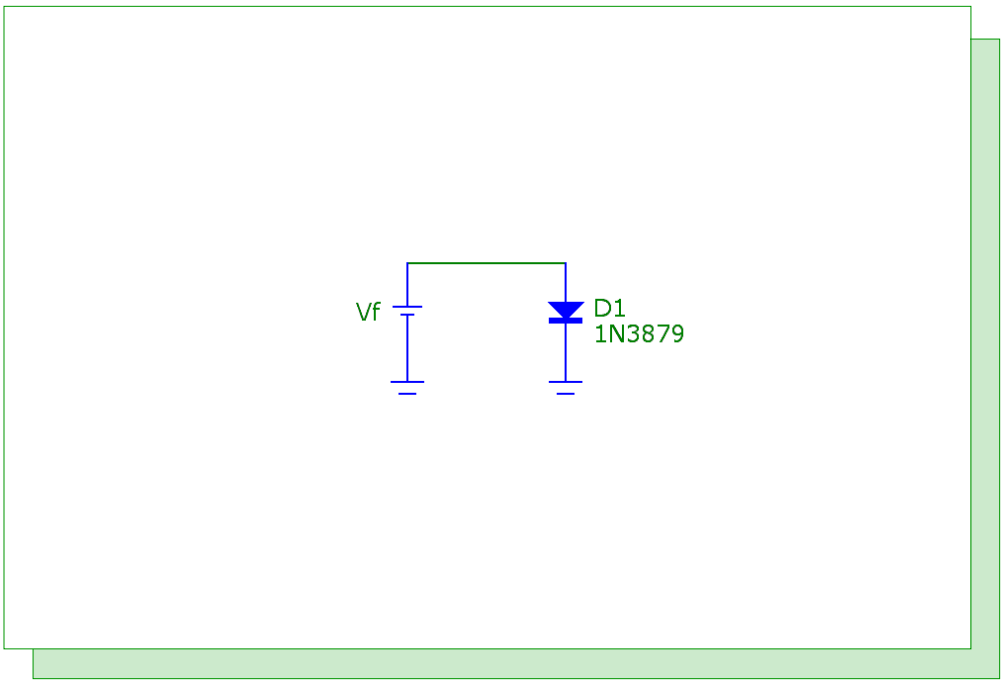


Fig. 2 - Diode If vs Vf schematic

To simulate the forward current versus forward voltage curve, the circuit is run in DC analysis. In the DC analysis limits, the Vf battery is swept linearly from .8V to 3.2V in increments of .01V. The Temperature field is set to run two branches of the simulation. One branch will be run at 150C. This will be the branch used to optimize the XTI, TRS1, and TRS2 model parameters. The second branch is run at 27C just to show the nominal curve of the 1N3879 diode.

The resulting DC simulation is shown below. The green curve is the branch when the temperature is set to 27C and provides an excellent match to the equivalent curve shown in the Motorola data book. The red curve is the branch when the temperature is set to 150C. This curve is a good deal off from the one specified in the data book which shows that the default temperature parameters in the model are not a good match for this device.

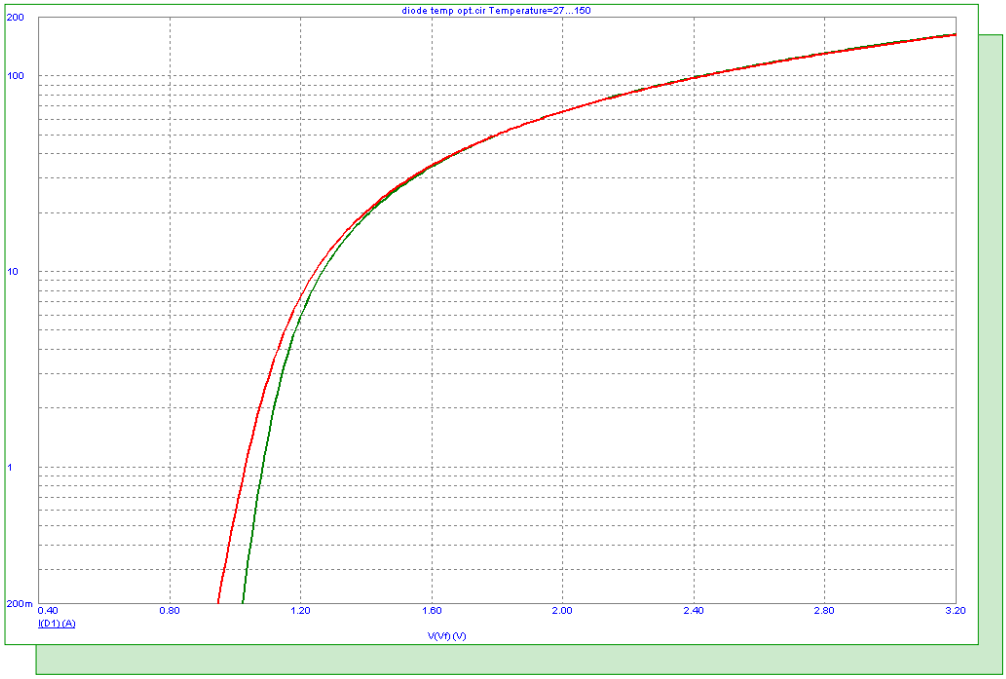


Fig. 3 - Unoptimized 150C curve and 27C curve

The circuit optimizer can now be used to derive better values for the 1N3879 temperature model parameters. To enter the optimizer, select the Optimize command in the DC menu. The settings in Figure 4 show the optimizer settings for the XTI, TRS1, and TRS2 parameters.

The Find section specifies the parameters that are to be optimized. All three parameters are setup to be optimized within the D1 component in the schematic. The parameter to be optimized can be selected by clicking on the Get button.

Since the object in this optimization is to match the forward current from the Motorola data book at 150C, the optimizing criteria in the That section for each function is set to Equates. This is the criteria that needs to be used for any curve fitting operation. A sampling of data from the data book for the curve at 150C is as follows:

@ Vf = .9, If = 1
@ Vf = 1, If = 2.5
@ Vf = 1.4, If = 15
@ Vf = 1.8, If = 30
@ Vf = 2.6, If = 58
@ Vf = 3.2, If = 81

The equivalent performance functions along with their To values that the optimizer needs to use to match to this data is:

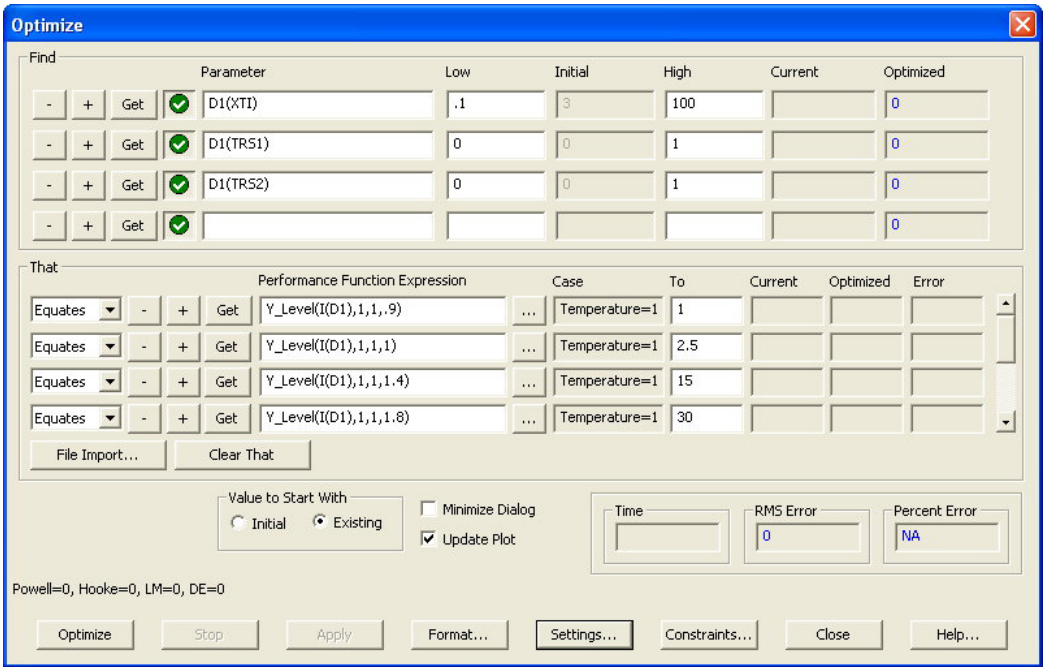


Fig. 4 - XTI, TRS1, and TRS2 optimizer settings

Function: Y_Level(I(D1),1,1,.9) To: 1
Function: Y_Level(I(D1),1,1,1) To: 2.5
Function: Y_Level(I(D1),1,1,1.4) To: 15
Function: Y_Level(I(D1),1,1,1.8) To: 30
Function: Y_Level(I(D1),1,1,2.6) To: 58
Function: Y_Level(I(D1),1,1,3.2) To: 81

For each of these functions, the Case field has been set to Temperature=150 in order to optimize the correct branch of the simulation. The Y_Level operator will try to optimize the Y value of the expression I(D1) at the specified X value to the value that is set in the To field. Since the X Expression in the DC Analysis Limits dialog box is set to V(Vf), the X value is the forward voltage across the diode. For example, with the first expression in the list, when the forward voltage is .9V, the optimizer will try to determine the values of XTI, TRS1, and TRS2 so that the forward current of the diode is equal to 1. Since six performance functions have been specified, the optimizer will find the values of XTI, TRS1, and TRS2 that produce the curve that creates the smallest total RMS error between the target and actual values at each point. Each of the Equates conditions are weighted equally in terms of importance when optimizing.

Clicking on the Optimize button initiates the optimization. The Powell optimization method finds the closest match to the specified data points. The optimizer has calculated a value for XTI of 14.241, a value for TRS1 of 21.779p, and a value for TRS2 of 78.095u. The values for these parameters produce a good match to the data book values having just a 3.7% error.

Clicking on the Apply button will update the diode model in the schematic so that the new XTI, TRS1, and TRS2 values are used. Applying the updated parameters from the optimizer does not actually overwrite the 1N3879 model in the Micro-Cap library file, but it localizes the model in the Models page of the schematic so that the changes only affect this specific circuit. The model statement could then be copied into the Micro-Cap library or copied into any other circuit file that would use the model. The updated model for the 1N3879 appears as follows:

.MODEL 1N3879 D (BV=50 CJO=107.82034563878P IBV=100.000001335143P
+ IS=4.641638012946F M=313.660097529485M N=1.255501899871 RL=6.04477627237MEG
+ RS=12.028656788586M TRS1=21.779p TRS2=78.095u TT=369.945519216272N
+ VJ=1.269832856815 XTI=14.241)

This model is a copy of the 1N3879 model from the Micro-Cap library with just different values for XTI, TRS1, and TRS2. Running the same schematic with the updated model statement produces the forward current versus forward voltage curves shown below. The green curve for the 27C branch has not changed at all. However, the red curve for the 150C now closely matches its equivalent curve from the Motorola data book.

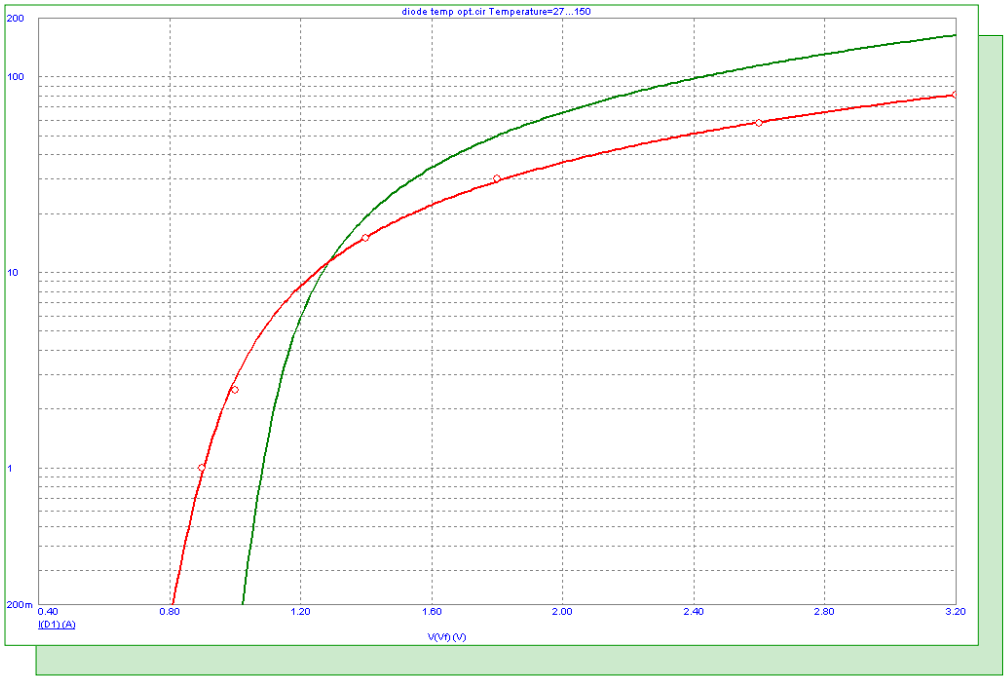


Fig. 5 - Optimized 150C curve and 27C curve

Simulating TDR Measurements

Time domain reflectometry (TDR) is a method by which a short duration pulse with a very fast rise time is injected into an electrical line in order to solve signal integrity issues. The reflected waveform from this pulse can be used to calculate the characteristics of the line such as the impedances and propagation delays along the signal path. This measurement can give a good indication of any discontinuites within the line that would occur with an open, short, or any other impedance mismatch.

Both of the examples used in this article were derived from the Maxim application note shown in Reference 1. The schematic shown below is used to demonstrate the basics of a TDR measurement. There are three separate circuits in the schematic. The only difference between the three is the value of the load resistance. The top circuit models a short at the line output. The middle circuit models an open at the line output. The bottom circuit models the case where the load impedance matches with the line impedance. A voltage source at the input to each of the circuits injects the fast rising pulse necessary to make the TDR measurement. Each of the voltage sources has its VALUE attribute defined as:

Pulse 0 2 0 25p 10n 1 4

This definition creates a 2 volt rising edge waveform with a rise time of 25ps. The width and period of the pulse are set to values high enough so that the falling edge of the pulse is not simulated. The source resistance in each circuit has been set at 50 ohms. The electrical line is modelled by a transmission line component whose VALUE attribute is:

TD=20n Z0=50

This creates an ideal transmission line that has a time delay of 20ns and a characteristic impedance of 50 ohms.

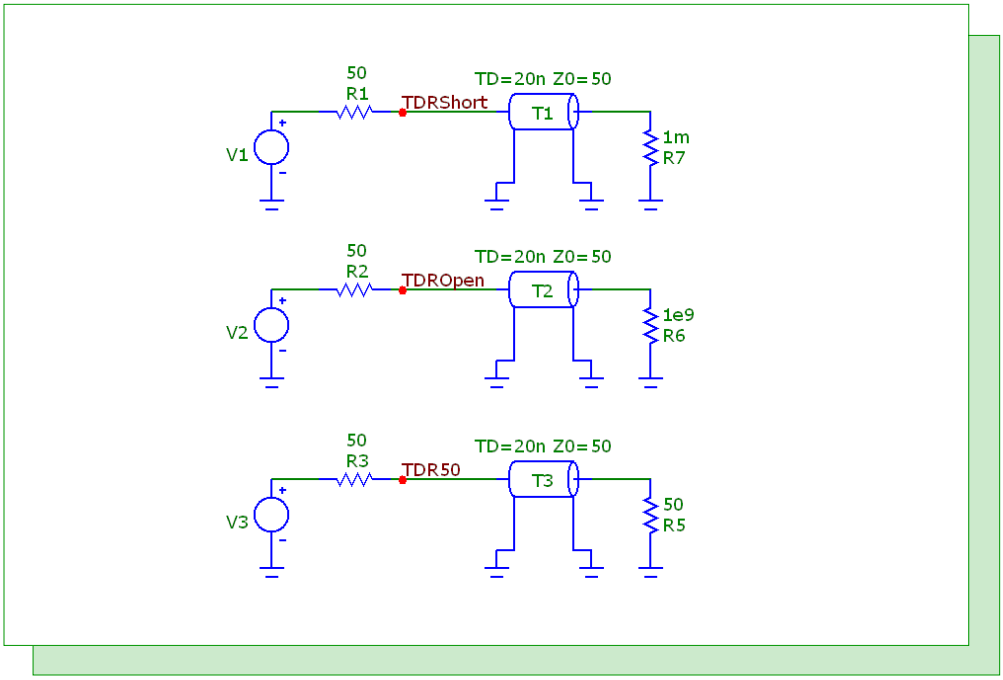


Fig. 6 - Basic TDR measurement circuit

The TDR measurement is run within a transient analysis. The simulation of the TDR measurements for each of the three circuits is displayed in the plots below. The simulation has been run for 100ns. The waveforms plotted are the voltages between the source resistances and the transmission line inputs. Since the time delay of the transmission line has been specified as 20ns, the reflected waveforms will appear after 40ns since the signal has to travel through the transmission line and back.

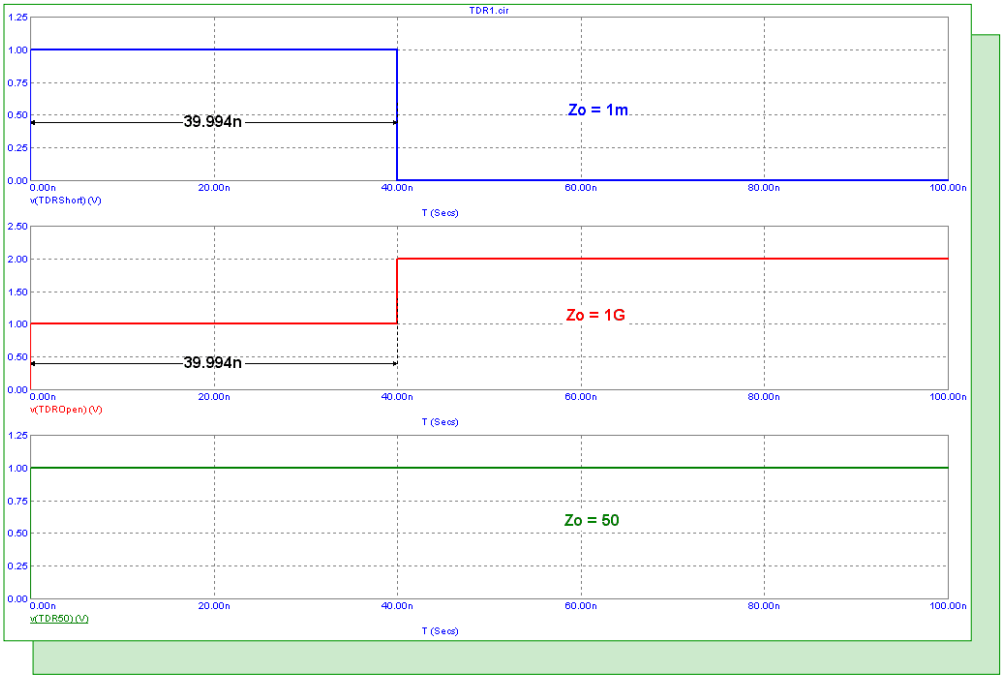


Fig. 7 - Basic TDR measurement waveforms

The top plot shows the TDR for the short circuit load. For a short circuit load, the reflected waveform is equal to the incident waveform but opposite in polarity so that the incident waveform is cancelled when the reflected waveform has propagated back through the transmission line at 40ns.

The middle plot shows the TDR for the open circuit load. For an open circuit load, the reflected waveform is equal to the incident waveform and has the same polarity so that the incident waveform is reinforced when the reflected waveform has propagated back through the transmission line at 40ns.

The bottom plot shows the TDR for the matched load. For a matched load, there is no reflected waveform, and the incident waveform is left intact.

The amplitude of the reflected waveforms can be used to calculate the impedances of the loads. The load impedance can be calculated from the following expression:

$$Z_L = Z_O * (1 + \rho) / (1 - \rho)$$

where Z_L is the load impedance, Z_O is the characteristic impedance and ρ is the reflection coefficient of the signal. This expression can be calculated within the analysis plot using the Formula capability of the analysis text. The following analysis text calculates the load impedance in each of the plots. The formula delimiters have been set as the square brackets, [ ].

Zo = [50*(1+(Y_Level(v(TDR50),1,1,50n)-1))/(1-(Y_Level(v(TDR50),1,1,50n)-1))]

The reflection coefficient is calculated by dividing the magnitude of the reflected waveform by the incident waveform. Since the incident waveform has a value of 1V in this example, the reflection coefficient can be calculated by measuring the magnitude of the waveform at a specific time and subtracting the incident waveform value to get the magnitude of the reflected waveform. The reflection coefficient is calculated in the above expression through the term:

Y_Level(v(TDR50),1,1,50n)-1

The Y_Level function returns the value of the voltage at node TDR50 at a time of 50ns. Subtracting one, which is the magnitude of the incident waveform, returns the magnitude of the reflected waveform. The formula analysis text in each plot correctly displays the value of the corresponding load resistor in the schematic.

The second example models the delay from an SMA edge connector to the DATA1 and NDATA1 input pins of a MAX9979 IC. The schematic is shown below. The V1 voltage source models the TDR input signal, and the R1 resistor is the TDR source resistance. The T1 transmission line models the test cable and has its VALUE attribute defined as:

ZO=50 td=1.5n

This gives the line a characteristic impedance of 50 ohms and a time delay of 1.5ns. The T2 and T3 lossy transmission lines model the PCB traces to the DATA1 and NDATA1 pins. Both of these traces are symmetrical and have identical lengths so the VALUE attribute for both transmission line components have been defined as:

LEN=.5 R=.01 L=130n C=30.5p

These values produce lines with a characteristic impedance of 65 ohms and a delay of approximately 1ns.

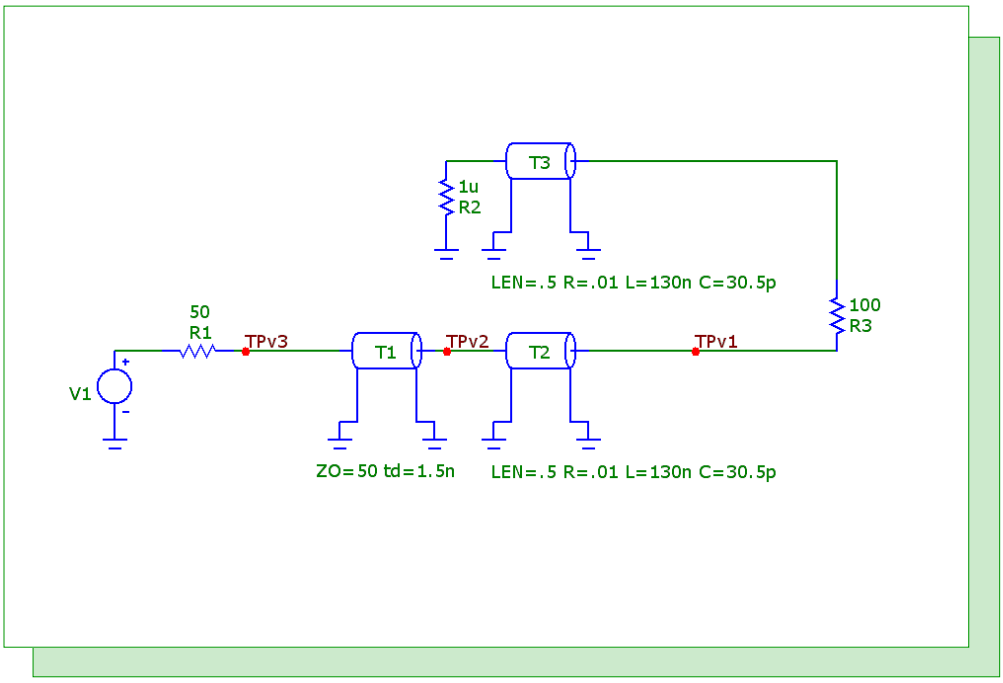


Fig. 8 - Maxim TDR measurement circuit

There is a 100 ohm resistor that goes between these two pins which is represented by R3. For this example, the NDATA1 pin has been terminated to ground.

The resulting transient analysis is shown below. The first reflected waveform occurs at 3ns which is twice the time delay of the test cable. Using the formula text described previously on this reflection calculates the impedance at approximately 65 ohms which matches the impedance of the T2 transmission line. This reflection lasts for 2ns which confirms the time delay of 1ns for the line. Secondary reflections occur at the test point as the signal settles down. The impedance calculation at the end of the simulation shows the 100 ohms from the R3 resistor.

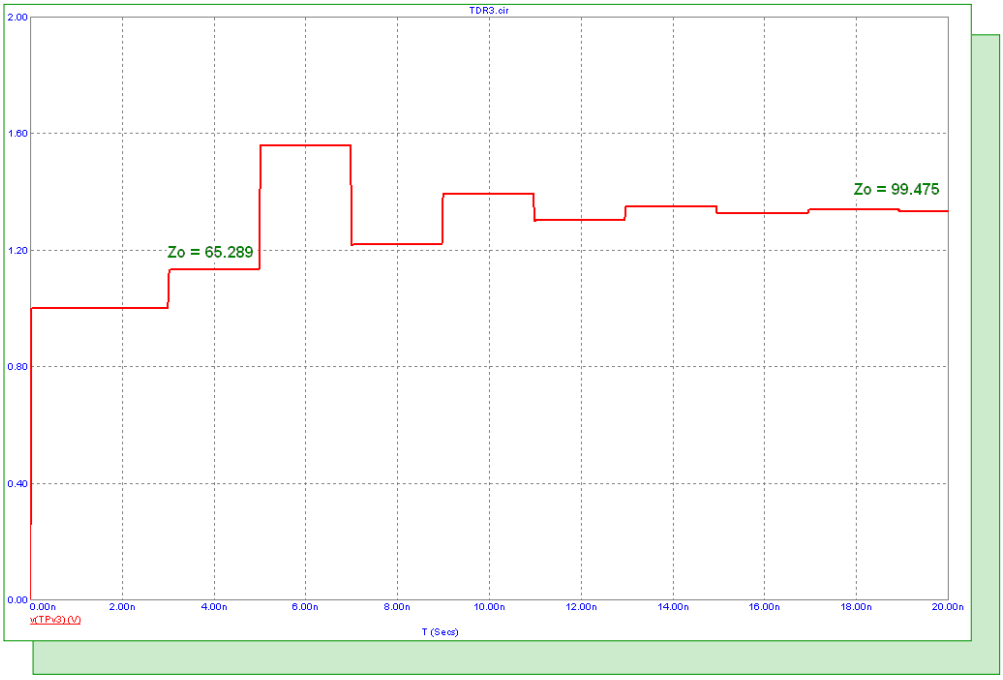


Fig. 9 - Maxim TDR measurement waveforms

Reference:
1) "Propagation Delay Measurements Using TDR", http://www.maxim-ic.com/app-notes/index.mvp/id/4395, Bernard Hyland, Maxim Application Note 4395

Measuring Power Factor in Linear Circuits

The power factor is the ratio of the real power used in the circuit to the apparent power in the circuit. When a load is completely resistive, the real power will be equal to the apparent power and the power factor will be 1. When reactances are present in the circuit, some of the energy will be stored in the circuit and then transferred back to the power source. This inefficiency increases the currents in the system which means that the apparent power in the circuit must be greater in order to consume the same amount of real power. A completely reactive circuit will consume no real power and the subsequent power factor will be 0. A low power factor results in greater distribution losses in the power system and should be avoided. For linear circuits, the power factor is also known as the displacement power factor.

The power factor can be measured in Micro-Cap through the use of the performance functions. The circuit below demonstrates a simple linear load that consists of an inductor and a resistor. The capacitor initially has its value set to 0 to act like an open circuit and will have its value optimized later for the power factor correction. A capacitor specified with a value of 0 will be entered into the SPICE matrix as 1e-100 farads which rarely, if ever, leads to convergence issues. The voltage source models a 120Vrms, 60Hz sine waveform.

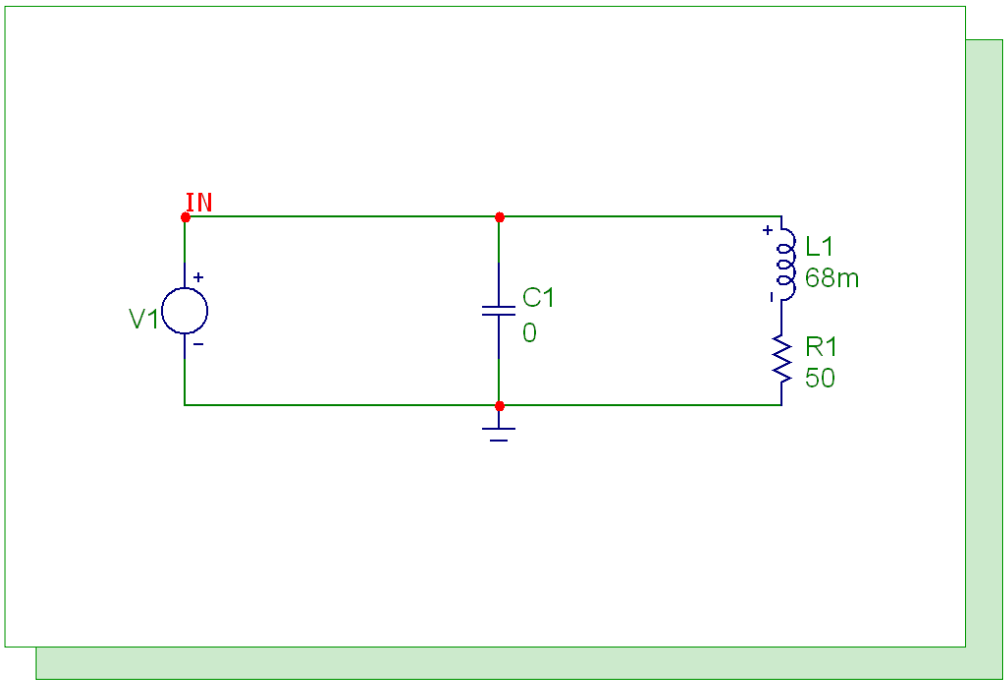


Fig. 10 - Power factor example circuit

The resulting transient analysis is shown in Figure 11. The top plot displays the voltage and current of the voltage source. The inductive load has caused the current to lag behind the voltage. The bottom plot displays the instantaneous power being generated by the voltage source. Note that the current has been specified as -I(V1) in order to display the current going into the circuit as a positive value. All three of these waveforms need to be plotted as they will all be used within performance functions in order to calculate the power factor.

The power factor is calculated through the use of performance functions within the analysis text of the bottom plot. The Formula capability within the analysis text is enabled with the square brackets, [ ], being used as the formula delimiters.

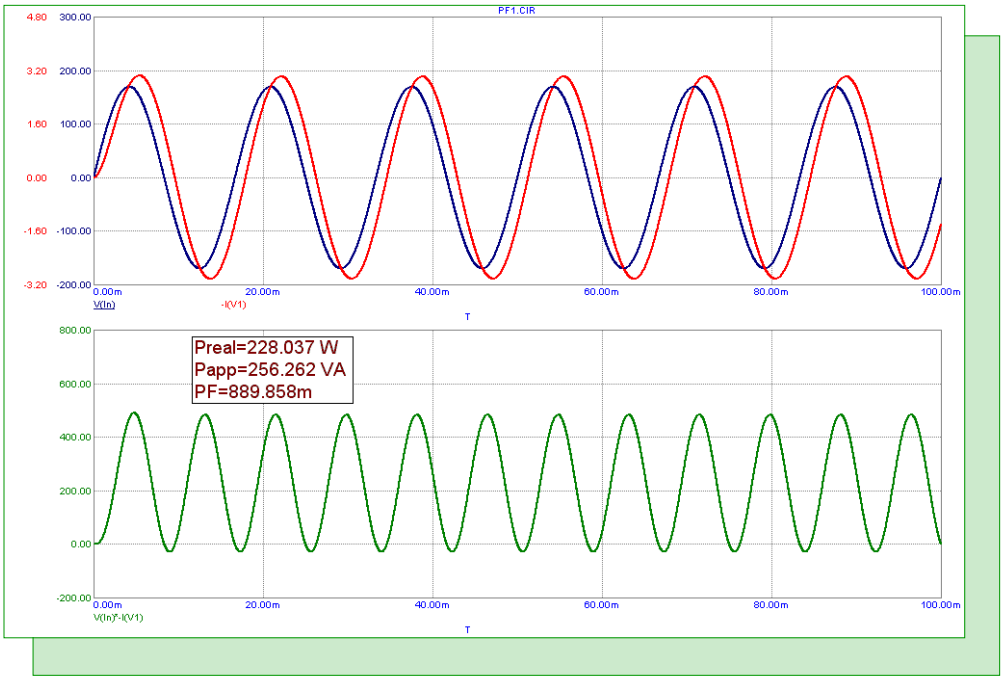


Fig. 11 - Power factor calculations

The real power of the circuit is calculated with the expression:

Preal=[Average(V(In)*(-I(V1)),1,50m,TMAX)] W

The expression between the square brackets calculates the average value of the instantaneous power from a range starting at 50ms to the end of the simulation. This range will exclude any initial transients. Periodic Steady State in the Transient Analysis Limits can also be used to simulate without initial transients. The apparent power of the circuit is calculated with the expression:

Papp=[RMS(V(In),1,50m,TMAX)*RMS(-I(V1),1,50m,TMAX)] VA

This expression multiplies the RMS value of the source voltage by the RMS value of the source current. Again, these are calculated starting from 50ms to the end of the simulation to exclude initial transients. Finally, the power factor is calculated by specifying the ratio of the above two expressions:

PF=[Average(V(In)*-I(V1),1,50m,TMAX)/(RMS(V(In),1,50m,TMAX)*RMS(-I(V1),1,50m,TMAX))]

These formulas return the following analysis text for this simulation:

Preal=228.037 W
Papp=256.262 VA
PF=889.858m

This load requires 256VA of apparent power from the power source in order to receive the 228W of real power that the circuit consumes. This produces a power factor of approximately .89. For linear circuits, there is a simple technique for improving the power factor. With an inductive load, placing a capacitor in parallel will correct a lagging power factor by drawing an equal but opposite amount of reactive power. Similarly, for a capacitive load, adding an inductor to the load would have the same effect.

The C1 capacitor shown in the schematic will be used to compensate for the lagging power factor. In order to determine a value for the capacitor to offset the reactive power of the inductive load, the Optimizer in Micro-Cap will be used. In the Transient menu, the Optimize command invokes the Optimizer dialog box shown below. In the Find section, the C1 component has been defined as the parameter to be optimized. The That section specifies that the capacitor optimization should try to equate the power factor expression to a value of 1. The power factor expression is the same one from the analysis text formula. Running an optimization shows that a capacitor with a value of approximately 21.5uF will produce the power factor correction for this circuit.

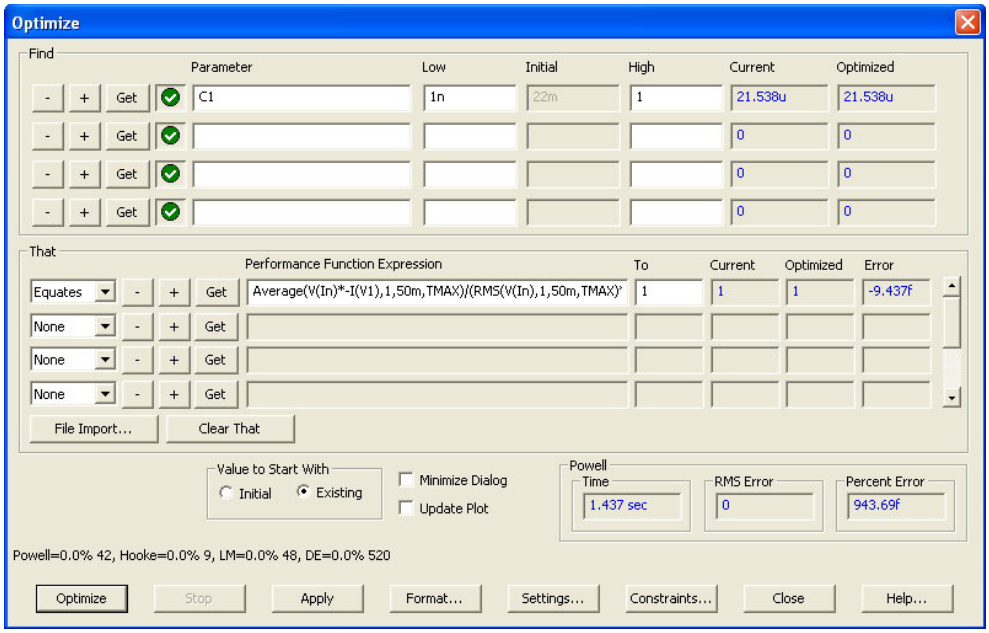


Fig. 12 - Power factor correction optimization settings

In the schematic, the capacitance has been rounded up to 22uF since that is a commonly available capacitor value. Running a transient analysis simulation on this modified circuit results in the plots shown in Figure 13. The addition of the capacitor has greatly improved the power factor. The top plot shows that the voltage and current from the source are now in phase. The analysis text in the bottom plot shows the power factor calculations of:

Preal=228.037 W
Papp=228.051 VA
PF=999.94m

The real power is unchanged from the previous simulation. However, the apparent power has been reduced to the point where it is essentially equivalent to the real power producing a power factor very close to 1.

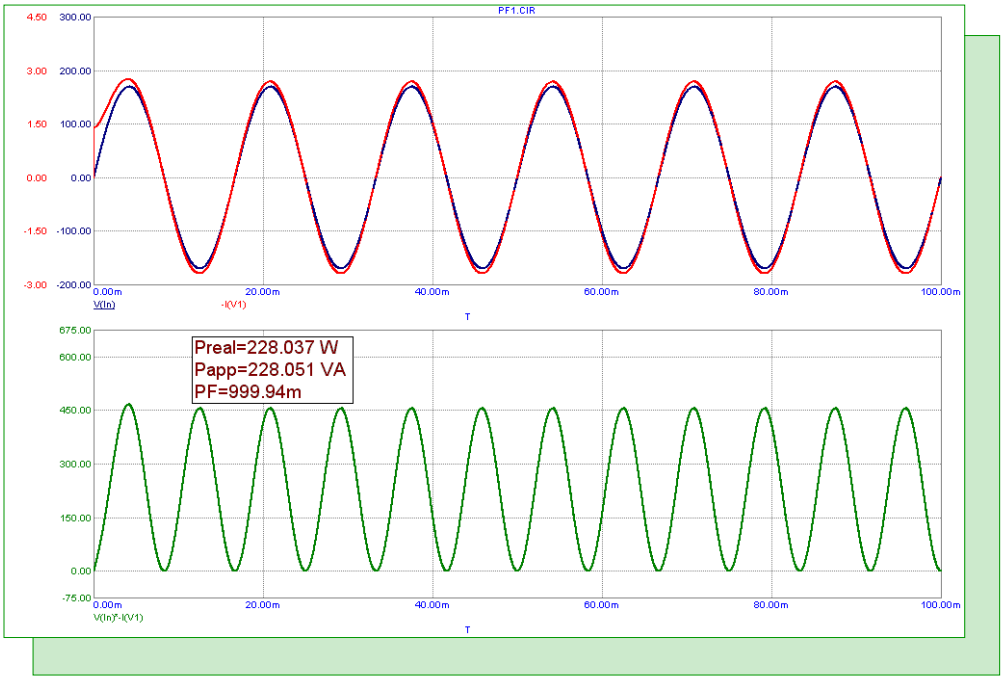


Fig. 13 - Power factor correction simulation

Product Sheet

Latest Version numbers

Micro-Cap 10 ..... Version 10.0.4
Micro-Cap 9 ..... Version 9.0.8
Micro-Cap 8 ..... Version 8.1.3
Micro-Cap 7 ..... Version 7.2.4

Spectrum's numbers

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