

Applications for Micro-CapTM Users

Summer 2009

News



Memristor Macros

Featuring:

- Memristor Macros
- Using the Tolerance Dialog Box
- Adding File Links to a Schematic

News In Preview

This newsletter's Q and A section describes how to capture images of the schematic and analysis plots in Micro-Cap for use in documentation. The Easily Overlooked Feature section describes the use of the Accumulate Plots option to easily compare plots created while editing the circuit in an analysis mode.

The first article describes new macro models that simulate the memristor which is the fourth elementary passive element (in addition to the resistor, capacitor, and inductor) that was first theorized about by Prof. Leon Chua in 1971 and finally developed recently by HP Labs.

The second article describes the use of the Tolerance dialog box as a means to quickly add, edit, or remove Monte Carlo tolerances for any of the applicable components in the schematic.

The third article describes how to add links to files directly in the schematic. This feature can be very useful when associating documentation such as application notes, design specifications, or manufacturer data sheets to a specific circuit.

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Book Recommendations

General SPICE

• Computer-Aided Circuit Analysis Using SPICE, Walter Banzhaf, Prentice Hall 1989. ISBN# 0-13-162579-9

• Macromodeling with SPICE, Connelly and Choi, Prentice Hall 1992. ISBN# 0-13-544941-3

• Inside SPICE-Overcoming the Obstacles of Circuit Simulation, Ron Kielkowski, McGraw-Hill, 1993. ISBN# 0-07-911525-X

• The SPICE Book, Andrei Vladimirescu, John Wiley & Sons, Inc., 1994. ISBN# 0-471-60926-9

MOSFET Modeling

• MOSFET Models for SPICE Simulation, William Liu, Including BSIM3v3 and BSIM4, Wiley-Interscience, ISBN# 0-471-39697-4

VLSI Design

• Introduction to VLSI Circuits and Systems, John P. Uyemura, John Wiley & Sons Inc, First Edition, 2002 ISBN# 0-471-12704-3

Micro-Cap - Czech

• Resime Elektronicke Obvody, Dalibor Biolek, BEN, First Edition, 2004. ISBN# 80-7300-125-X

Micro-Cap - German

• Schaltungen erfolgreich simulieren mit Micro-Cap V, Walter Gunther, Franzis', First Edition, 1997. ISBN# 3-7723-4662-6

Micro-Cap - Finnish

• Elektroniikkasimulaattori, Timo Haiko, Werner Soderstrom Osakeyhtio, 2002. ISBN# 951-0-25672-2

Design

• High Performance Audio Power Amplifiers, Ben Duncan, Newnes, 1996. ISBN# 0-7506-2629-1

• Microelectronic Circuits, Adel Sedra, Kenneth Smith, Fourth Edition, Oxford, 1998

High Power Electronics

• Power Electronics, Mohan, Undeland, Robbins, Second Edition, 1995. ISBN# 0-471-58408-8

• Modern Power Electronics, Trzynadlowski, 1998. ISBN# 0-471-15303-6

Switched-Mode Power Supply Simulation

• SMPS Simulation with SPICE 3, Steven M. Sandler, McGraw Hill, 1997. ISBN# 0-07-913227-8

• Switch-Mode Power Supplies Spice Simulations and Practical Designs, Christophe Basso, McGraw-Hill 2008. This book describes many of the SMPS models supplied with Micro-Cap.

Micro-Cap Questions and Answers

Question: I am creating documentation for my circuit, and I would like to use graphic captures of the schematic and simulations within the documentation. Is there a way to create picture files within Micro-Cap so I can easily import these images into my documentation?

Answer: There are two methods for capturing the schematic and analysis plots to a graphic image. These images can either be copied to the Windows clipboard to paste in another program, or they can be saved to a file on the hard drive which can then be imported into another program.

In order to copy an image into the Windows clipboard, the group of commands available in the Copy to Clipboard section of the Edit menu may be used. These command are as follows:

Copy the Visible Portion of Window in BMP Format: This command copies the visible portion of the active window to the Windows clipboard in BMP format.

Copy the Select Box Part in BMP Format: This command copies the portion of the schematic that is enclosed within the select box to the Windows clipboard in BMP format. Only the portion of the select box that is visible in the active window will be copied.

Copy the Entire Window in WMF Format: This command copies all contents of the active window to the Windows clipboard in Windows Metafile format.

Copy the Entire Window in EMF Format: This command copies all contents of the active window to the Windows clipboard in Enhanced Metafile format.

The second possibility is to create a picture file through the Copy the Entire Window to a Picture File command available in the Edit menu. This command creates a picture file in one of many available formats from the front window. The file can then be imported into Micro-Cap or other Windows applications. The picture formats that are available are: BMP, JPEG, GIF, EMF, WMF, TIFF, and PNG.

Easily Overlooked Features

This section is designed to highlight one or two features per issue that may be overlooked among all the capabilities of Micro-Cap.

Accumulate Plots option

The Accumulate Plots option is an option that is available within the Transient, AC, DC, and Distortion Analysis Limits dialog boxes. When enabled, this option accumulates waveforms or curves that result from editing the circuit while still in the analysis mode. It provides a simple method to compare the results of a circuit before and after editing. There is no limit to the number of analysis runs that can be accumulated. Exiting the analysis mode clears all of the data.

The sample circuit PRLC.CIR is used to demonstrate how this option works. Once the circuit is loaded, the Transient Analysis command is selected under the Analysis menu. In the Transient Analysis Limits dialog box, the Accumulate Plots option is enabled. The analysis is then run. While still in the analysis, the circuit window is activated, and the inductor value is changed to 2uH. The circuit is simulated again. Both simulations are now available in the plot window for easy comparison as shown in the figure below.



Fig. 1 - Accumulate Plots enabled analysis

The Dynamic Auto Run option in the Preferences - Options - Analysis section forces a new simulation run every time an edit is made in the circuit while in an analysis. If more than one edit needs to be made prior to a simulation, this option needs to be disabled. In this case, once all the edits are made, the simulation would need to be manually started by the user by hitting F2 or using the Run command.

The Clear Accumulated Plots under the Scope menu will clear all of the prior runs the next time a simulation is started. The toolbar icon for this command is the following:



Memristor Macros

The memristor device is the fourth elementary passive element (in addition to the resistor, capacitor, and inductor) that was first theorized about by Prof. Leon Chua in 1971 and finally developed recently by HP Labs. The resistance of the memristor will change depending on the flow of charge for the device. If the charge flows in one direction, the resistance of the device increases. If the charge flows in the other direction, the resistance of the device decreases. The key to the memristor is that when the flow of charge stops, the device remembers the last resistance it was at, so that when the flow of charge resumes, the device also resumes operation at the previous resistance. The memristor has great potential for low power, high density memory applications.

Prof. Dalibor Biolek, who helped develop a SPICE model for the memristor (Reference 1), has generously supplied Spectrum Software with a couple of memristor macros along with four test circuits which are in Micro-Cap 9 format. The files are available in the Summer 2009 section of our Newsletter page on the website.

The first memristor macro (Memristor_J.Mac) uses the Joglekar window function which is the conventional model for simulating the nonlinear dopant drift of a memristor. Driving this memristor macro with a 1.2V, 1Hz sinusoidal voltage produces the transient simulation shown below.



Fig. 2 - Driving the memristor with a sinusoidal voltage

The top plot shows the relation between the charge and the flux of the memristor which demonstrates the one-to-one correspondence between the two as expected in memristor theory. The second plot shows the hysteresis loops within the I-V curves of the memristor. Increasing the frequency of the driving sinusoidal voltage will gradually suppress the hysteresis curves. The third plot displays the voltage and current waveforms of the memristor in the time domain. The bottom plot shows the ratio of the actual width of the doped area to the width of the entire memristor thin film. In this simulation, the ratio does not approach the boundary limits where the dominant nonlinear effects occur. Lowering the Roff/Ron ratio of the memristor and increasing the sinusoidal voltage to 2V produces a simulation that displays the hard switching case. The transient simulation for this configuration is shown below. This simulation was run a few times with the State Variables option set to Leave in order to reach the steady state operation.



Fig. 3 - Hard switching memristor simulation

The same plots from the previous simulation are plotted again. As can be seen in the bottom plot, the hard switching occurs when the ratio of the width of the doped region to the width of the memristor is switched between the low and high boundary limits. The corresponding nonlinear effects of the hard switching can be seen in the current plots of the memristor.

The second memristor macro (Memristor_B.Mac) uses the Biolek window function for simulating the nonlinear dopant drift. The Joglekar window function used in the first macro file models the ideal memristor properties. However, this window function can have problems when the memristor is operated under some hard switching conditions. When the memristor is driven to its Ron or Roff values, the Joglekar window function can lock in on that state with no means to drive it back to normal operation. The Biolek window function includes some nonideal factors and suppresses the memory effect on the boundary states to more accurately model the probable real life operation of the device.

In order to compare the boundary effects of the two window functions, each type of memristor is driven by an identical 1.6mA current pulse source. The transient analysis results of this simulation is displayed in Figure 4.

The waveforms in the top plot show the voltage and current waveforms for the memristor macro that uses the Joglekar window function. Once the driving current becomes large enough to switch the memristor into one of its boundary states, the memristor locks into that state and no external stimulus can change the memristor back to another resistance value. The waveforms in the middle plot show the voltage and current waveforms for the memristor macro that uses the Biolek window function. Even though the memristor is being driven with the same current, it is not being locked into either boundary state which is the expected operation of an actual memristor.

The waveforms in the bottom plot shows the ratio of the actual width of the doped area to the width of the entire memristor thin film for both memristor macros. The V(XJ.X) waveform plots the ratio for the memristor using the Joglekar window function, and the V(XB.X) waveform plots the ratio for the memristor using the Biolek window function. For the Joglekar plot, the waveform locks into the 0 state after the first current pulse and no longer reacts to any of the following current pulses.



Fig. 4 - Joglekar versus Biolek window functions

The Memristor_J macro provides a macro that will simulate according to the ideal memristor theory whereas the Memristor_B macro tries to incorporate a little more of the real world effects that a memristor may have.

Reference:

[1] BIOLEK, Z., BIOLEK, D., BIOLKOVA, V. "SPICE model of memristor with nonlinear dopant drift." Radioengineering, 2009, vol. 18, no. 1. http://www.radioeng.cz/fulltexts/2009/09_02_210_214.pdf

Using the Tolerance Dialog Box

Setting tolerances is typically done in the Attribute dialog box or by directly editing the model in the schematic file. If many tolerances need to be defined, this can become a tedious process. Micro-Cap provides the Tolerance dialog box as a means to quickly add, edit, or remove tolerances for any of the applicable components in the schematic. The dialog box appears as below.

| The Dialog of Tolerance Types NPN | Models | Parameters |
|---|-------------------------------|--|
| PULSE RESISTOR | N2 (Q2,Q6) | BF=250 BR=1 CJC=0.8P CJS=0 EG=1.11 FC=500m IKF=0 IKR=0 IKR=0 IS=.1f ISC=0 ▼ |
| Select All Clear All | Select All Clear All | Select All Clear All |
| LOT | DEV | Tolerance Sets |
| C Add/Change C Leave C Remove | C Add/Change C Leave C Remove | Save |
| Lot# Distribution Tolerance None DEFAULT | Lot# Distribution Tolerance | Apply Delete |
| Apply Format OK Cancel Help | | |

Fig. 5 - Tolerance dialog box

The Tolerance dialog box, which is accessible from the Monte Carlo dialog box and also from the Change submenu under the Edit menu, lets you apply tolerances to multiple parameters at once. You can apply LOT and DEV tolerances to any part that has a model statement. You can also save Tolerance sets for later use on other models of the same type. The dialog box has these fields:

Types: This list the parts types found in the circuit. You can select one or more types for tolerancing, although only one type is usually selected.

Models: This lists each model found for the selected part type(s). You can select one or more models for tolerancing. For resistors, capacitors, and inductors, if the Model attribute has not been specified in the schematic, the part will still appear in this list but be preceded by a <Blank> designator. If selected for tolerancing, Micro-Cap will prompt for a model name to assign the selected part(s) along with the subset of parts from that entry to apply the model to.

Parameters: This lists the model parameters for each selected model. Select the parameters that are to be toleranced. Use the Ctrl or Shift keys to select multiple parameters.

Lot: This controls the options for the Lot tolerance.

Add/Change: This adds or changes the Lot tolerance of the selected parameter(s) to the value in the Tolerance field, when the Apply button is clicked.

Leave: This option leaves the Lot tolerances unchanged.

Remove: This option removes the Lot tolerance of the selected parameter(s).

Lot#: This field lets you enter a lot # for the Lot tolerance to provide a means for lot deviations to track one another.

Distribution: This lets you select the type of distribution. Default means that the model will use the distribution setting from the Monte Carlo Options dialog box.

Tolerance: This field lets you enter the tolerance. You can enter an absolute tolerance or a percentage tolerance. For a percentage tolerance, you must specify the % symbol.

Dev: This controls the options for the Dev tolerance. The options are the same as for the Lot tolerance above.

Tolerance Sets: This lets you assign a name to a tolerance set so it can be used for other parts of the same model statement type. To name a set, click on Save and enter a name, such as 60n_MOS-FET or Caps_5%. This will save the tolerance settings on the current parameter list so any tolerances must first be applied to the parameters before saving. To apply a tolerance set to the selected parameters, select the set name from the list and click on Apply. To delete a tolerance set, select the name of the set to be removed, then click on the Delete button.

As an example of how the Tolerance dialog box works, the circuit Diffamp.cir will be used. This circuit is distributed with Micro-Cap. The Tolerance dialog box is invoked through the use of the CTRL+SHIFT+T hotkey command. The three types of components that have models to tolerance in the Diffamp.cir file are shown in the Types field: NPN, PULSE, and RESISTOR. First, a 10% LOT tolerance will be applied to the BF, CJC, and CJE parameters of the N2 NPN model. The NPN item is selected in the Types field. Once selected, all of the available NPN models in the circuit are then displayed in the Models field. The N2 model is specified in the Models field as:

N2 (Q2, Q6)

which means that the N2 model is being used by the transistors with the part names Q2 and Q6 in the schematic. Selecting the N2 line in the Models field will then display all of the applicable model parameters in the Parameters field. Holding the CTRL key down, the BF, CJC, and CJE parameters are all clicked on in the Parameters field in order to select them. In the Lot section, the Add/ Change option is selected. A value of 10% is entered into the Tolerance field. Since only a Lot tolerance is going to be added to these parameters, in the Dev section, the Leave option is selected so that no changes occur to any Dev tolerances. The Tolerance dialog box should now appear as it does in Figure 6. Clicking Apply will change the model in the schematic file and update the corresponding parameters in the Parameters field.

For the next step, all of the resistors in the schematic will have a 5% Lot tolerance added to them. In the Tolerance dialog box, the RESISTOR item is selected in the Types field. In the Models field, the following line appears:

<black> (R1,R4,R2,R5,R6,R3,R7,R10,R9,R8)

In the Diffamp.cir file, there are ten resistors, and none of them have a model assigned to them. However, in order to tolerance a resistor, a model must be assigned to the component. The <blank> designation allows resistors without models to be selected in this dialog box. Once the above line is selected, the applicable resistor model parameters are displayed in the Parameters field. In order to tolerance a resistance, the R model parameter should have the Lot tolerance applied to it

| rpes | Models | Parameters |
|-----------------------------|--------------------------------|----------------------|
| IN ISE | N1 (Q1,Q3,Q4,Q5) N2 (Q2,Q6) | AF=1 BE=50 |
| ESISTOR | 110 ((2)) | BR=1 |
| | | CJC=1P |
| | | CIE=2P CIS=0 |
| | | EG=1.11 |
| | | FC=500m |
| | | |
| | | IRB=0 |
| | | IS=.1f |
| Select All Clear All | Select All Clear All | Select All Clear All |
| т | DEV | Tolerance Sets |
| Add/Change C Leave C Remove | C Add/Change 🕞 Leave C Remove | Save |
| ot# Distribution Tolerance | Lot# Distribution Tolerance | Apply |
| Ione VIDEFAULT VI 10% | None V DEFAULT | Delete |

Fig. 6 - Tolerancing the N2 NPN model

so the R parameter is selected in the Parameters field. Now the same technique used with the NPN model parameters can be used to tolerance the R parameter. However, the resistor also has four tolerance sets available to it: E12, E24, E48, E96. The tolerance sets provide predefined tolerance values that can be easily applied to the selected model. For the resistor, these four sets tolerance the R parameter as follows:

E12 - 10% E24 - 5% E48 - 2% E96 - 1%

In order to set the resistance tolerances to 5%, the E24 entry is selected from the Tolerance Sets list. The dialog box should appear as it does in Figure 7. Next, the Apply button that is within the Tolerance Sets section is clicked. This applies the 5% tolerance for the R parameter stored in the E24 set to the selected resistor models.

Since the resistors that were selected in the Models field did not have any model assigned to it previously, the Assign Model dialog box shown in Figure 8 will be invoked when the Apply button is clicked. In the Model Name field, a name needs to be entered. In this case, the name RMod will be used. The next step is to select which of the resistors that this model will apply to. Since all of the resistors are to be toleranced, all the entries in the dialog box are selected, and the OK button is clicked.

At this point, all of the selected resistors will then have their MODEL attribute set to the specified model name RMod. Also, the following model statement is created in the Models page of the schematic.

.MODEL RMOD RES (R=1 LOT=5%)

Clicking the OK button in the Tolerance dialog box will then make all the changes permanent.

| The Dialog of Tolerance Types NPN PULSE RESISTOR | -Models <blank> (R1,R4,R2,R5,R6,R3,R7,R10,R9,R</blank> | Parameters CP=undefined LS=undefined NM=1 T_ABS=undefined T_REL_SLOEAL=undefined T_REL_LOCAL=undefined TCI=0 TCE=0 |
|--|--|--|
| Select All Clear All | Select All Clear All | Select All Clear All |
| LOT | DEV | Tolerance Sets |
| Add/Change C Leave C Remove Lot# Distribution Tolerance None DEFAULT 10% | C Add/Change C Leave C Remove Lot# Distribution Tolerance None DEFAULT V | E12 E24 E48 E96 Delete |
| Apply Format OK Cancel Help | | |

Fig. 7 - Tolerancing the resistors

| Assign Model | × |
|---|---|
| Model Name Select Components to assign model to | |
| R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 | |
| OK Cancel Help | |

Fig. 8 - Assign Model dialog box

Adding File Links to a Schematic

Micro-Cap has the capability to add links to files directly in the schematic. This feature can be very useful when associating documentation such as application notes, design specifications, or manufacturer data sheets to a specific circuit. File links can reference a file on the local system or use a URL to access a file on the Internet. There are two methods that can be used to implement file links. The link can be specified either through schematic grid text or through the Link field of a component within the Component Editor. Once the links have been specified, the File Link mode can then be used to open the assigned files from the schematic.

Using Grid Text

The Text mode in the schematic can be used to add a file link as a text string to a schematic page. When entering the text, only the actual path and file name should be in the string. Any other text describing the link would need to be entered through a separate text entry. For example, if you were to enter a link to the Micro-Cap 9 User's Guide PDF file, you could enter the following string:

C:\MC9\DOCUMENTS\UG.PDF

Note that for files on the local system, if the path is not specified, it will use the path specified in the Document field within the Paths dialog box. The Paths dialog box can be accessed under the File menu. In a similar manner, the internet URL of a file can also be specified. For example, if you were to enter a link to Spectrum Software's website, you would enter the following string:

http://www.spectrum-soft.com

Both of these would just appear as standard grid text in the schematic. These strings can always be modified by the user, such as adding an underline to the string to give it the hyperlink look, by just double clicking on the text string in Select mode. This invokes the Grid Text dialog box where you can edit the string and its properties.

To open a file link, the File Link mode needs to be activated. This can be done by selecting File Link under the Mode section of the Options menu, or by clicking on the following icon in the toolbar.

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Once in File Link mode, simply click on the text string in the schematic, and the file will be opened.

Using the Component's Link field

Each component in the Component library can have a file link associated with it. The main use of this feature is to link a data sheet or an application note to a specific device although any type of web page or file can be linked to a component.

The file link for a component is defined within the Link field in the Component Editor. The Component Editor is accessible under the Windows menu. The Link field can also reference either a file on the local system or an internet URL.

The file link is globally defined so it is available for all instances of the component. When the component is placed in a schematic, there are two methods to access the linked file. One method is to enable File Link mode. Once this mode is enabled, simply click on an instance of the component in the schematic to open the corresponding file. The second method is to double click on the component when in Select mode to invoke the Attribute dialog box. Below the two rows of buttons is hyperlinked text that states File Link. Clicking on this link will also open up the associated file. If either of the above methods is done with a component that does not have an entry in the Link field in the Component Editor, Micro-Cap will use the default path defined in the File Link Default field in the Preferences / Options / Circuit page. The default link is initially set to perform a Google search on the part name and the phrase "data sheet".

Components can be created whose only function is to provide a file link. This is useful if the same documentation is to be used across multiple circuits, and it can also provide a better visual display versus using the grid text file link. One example of such a component has its Component Editor settings displayed in the figure below.



Fig. 9 - Document component in the Component Editor

In this case, a component was created to provide a link to Spectrum Software's Newsletters page. The name was defined as "Spectrum News". The name should be descriptive to the user, but it does not have an effect on the actual operation of the device. The shape chosen for the part is called Document. This shape is in Micro-Cap's standard shape library and looks like a page. The definition of the component is set to Blank. The Blank definition defines a component that has no electrical properties and is simply used for documentation purposes. Finally, the Link field for the component is defined with the URL to the Newsletter section as:

http://www.spectrum-soft.com/news.shtm

The Test button next to the Link field can be used to test the link to make sure it is pointing at the correct file. This part will now be available to enter into any schematic. A schematic that contains this component along with a couple of grid text file links is shown in the figure below.



Fig. 10 - Example circuit containing file links

Product Sheet

Latest Version numbers

| Micro-Cap 9 | Version 9.0.6.1 |
|-------------|-----------------|
| Micro-Cap 8 | |
| Micro-Cap 7 | Version 7.2.4 |

Spectrum's numbers

| Sales | (408) 738-4387 |
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