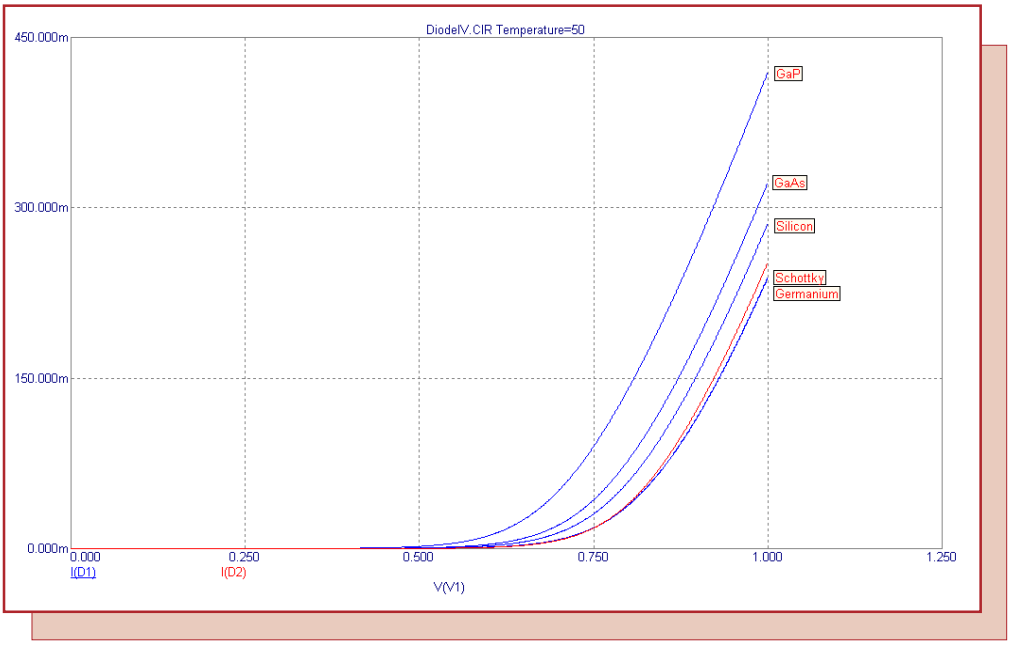
spectrum news

Applications for Micro-Cap™ Users

Summer 2003

News



Diode Material Temperature Parameters

Featuring:

- Creating A Schmitt Trigger Input Digital I/O Interface Model
- Smooth Transition Time Switch
- Diode Materials Temperature Parameter Values

News In Preview

This newsletter's Q and A section describes the different pin display options available within the Attribute dialog box. The Easily Overlooked Features section describes the Clear Cut Wire command that can be used when deleting areas of the circuit.

The first article describes the process of creating a new Schmitt trigger input digital I/O interface model for the 74LV-A family.

The second article describes how to create a smooth transition time switch in order to aid convergence.

The third article describes the values for the diode temperature parameters that must be set in order to model diodes using semiconductor materials other than silicon.

Contents

Book Recommendations

General SPICE

• *Computer-Aided Circuit Analysis Using SPICE*, Walter Banzhaf, Prentice Hall 1989. ISBN# 0-13-162579-9

• *Macromodeling with SPICE*, Connelly and Choi, Prentice Hall 1992. ISBN# 0-13-544941-3

• *Inside SPICE-Overcoming the Obstacles of Circuit Simulation*, Ron Kielkowski, McGraw-Hill, First Edition, 1993. ISBN# 0-07-911525-X

• *The SPICE Book,* Andrei Vladimirescu, John Wiley & Sons, Inc., First Edition, 1994. ISBN# 0-471-60926-9

MOSFET Modeling

• *MOSFET Models for SPICE Simulation, William Liu, Including BSIM3v3 and BSIM4*, Wiley-Interscience, First Edition, ISBN# 0-471-39697-4

VLSI Design

• *Introduction to VLSI Circuits and Systems,* John P. Uyemura, John Wiley & Sons Inc, First Edition, 2002 ISBN# 0-471-12704-3

Micro-Cap - German

• *Schaltungen erfolgreich simulieren mit Micro-Cap V,* Walter Gunther, Franzis', First Edition, 1997. ISBN# 3-7723-4662-6

Micro-Cap - Finnish

• *Elektroniikkasimulaattori,* Timo Haiko, Werner Soderstrom Osakeyhtio, 2002. ISBN# ISBN 951-0-25672-2

Design

• *Microelectronic CircuitsHigh Performance Audio Power Amplifiers,* Ben Duncan, Newnes, First Edition, 1996. ISBN# 0-7506-2629-1

• *Microelectronic Circuits.,* Adel Sedra, Kenneth Smith, Fourth Edition, Oxford, 1998

High Power Electronics

• *Power Electronics,* Mohan, Undeland, Robbins, Second Edition, 1995. ISBN# 0-471-58408-8

• *Modern Power Electronics,* Trzynadlowski, 1998. ISBN# 0-471-15303-6

Switched-Mode Power Supply Simulation

• *SMPS Simulation with SPICE 3,* Steven M. Sandler, McGraw Hill, First Edition, 1997. ISBN# 0-07-913227-8

• *Switch-Mode Power Supply SPICE Simulation Cookbook*, Christophe Basso, McGraw-Hill 2001. This book describes many of the SMPS models supplied with Micro-Cap.

Micro-Cap Questions and Answers

Question: I have been experimenting with some of the display options that are available in the Attribute dialog box. There are three options that refer to the pins of the component: Pin Markers, Pin Names, and Pin Numbers. What is the purpose of each of these?

Answer: Each of these options will either enable or disable the display of a particular pin specification. They work as follows:

Pin Markers: This display option controls the display of markers showing the location of the pin connection points. The markers show the actual point where any components or wires must connect to in order to be electrically wired to the component for the simulation. When enabled, the pin connection points will be marked by small filled circles.

Pin Names: This display option controls the display of the pin names that have been assigned to the component. The names displayed are the pin names that have been assigned to the particular component within the Component Editor. Displaying the pin names can be useful for a number of components in the analog and digital libraries whose shape doesn't symbolize the function of each of the pins for the component.

Pin Numbers: This display option controls the display of the package pin numbers. The numbers displayed are the package numbers that have been assigned to each of the component's pins within the Package Editor. The package pin numbers are only used in Micro-Cap when performing a translation to a PCB netlist file. While the Pin Markers and Pin Names can be displayed for any component within Micro-Cap, enabling the Pin Numbers option will only display the pin numbers when the following qualifications have been met.

1) At least one package has been defined for the specific component in the Package Editor. Most of the analog and digital libraries have had packages defined in the default installation of Micro-Cap. In the Attribute dialog box, any available packages can be seen by highlighting the PACKAGE attribute, and then clicking on the drop down arrow at the end of the Value field.

2) The PACKAGE attribute for the component has been assigned one of the package names that was defined for the component within the Package Editor.

3) If after defining the PACKAGE attribute, GATE and COMPNAME attributes appear in the Attribute dialog box, the GATE attribute must be defined also. This will occur when multiple instances of the component are available within the package such as with the 7400 component. Highlighting the GATE attribute and clicking the drop down arrow at the end of the Value field will display the possible definitions for the attribute.

Easily Overlooked Features

This section is designed to highlight one or two features per issue that may be overlooked because they are not made visually obvious with a toolbar button.

Clear Cut Wire (CTRL + DELETE)
The common method for deleting multiple objects in a schematic is to drag a select box over the area that is to be deleted. The select box will highlight any components, wires, text, and objects that fall within the drag area. For wires, if even a small portion of the wire segment is within the select box, the entire wire segment will be highlighted. In Figure 1, the select box has been drawn to delete the three batteries. Note that for the three wires, the entire wire segment has been selected.

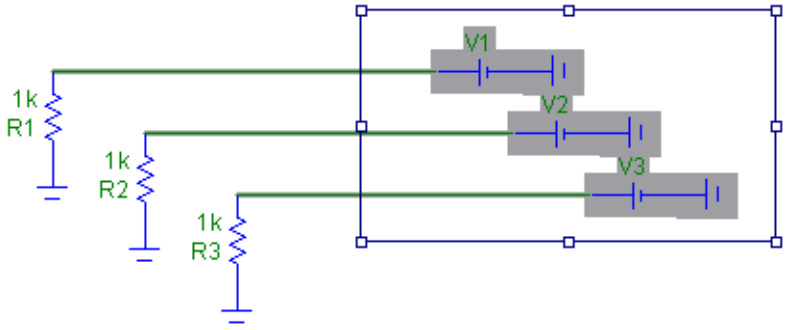


Fig. 1 - Schematic After Select Box Drag

Now if the Clear command is chosen or the Delete key hit, the wire segments will be completely deleted, and only the resistors will be left in the circuit. In some cases, it may not be desirable to have the entire wire deleted. For these instances, the Clear Cut Wire command is available under the Edit menu. This command deletes selected wires by cutting them exactly at the sides of the select box. The CTRL+DELETE hotkey combination may also be used. Figure 2 shows the result after the Clear Cut Wire command has been invoked. The wire segment outside of the select box has remained in the schematic.

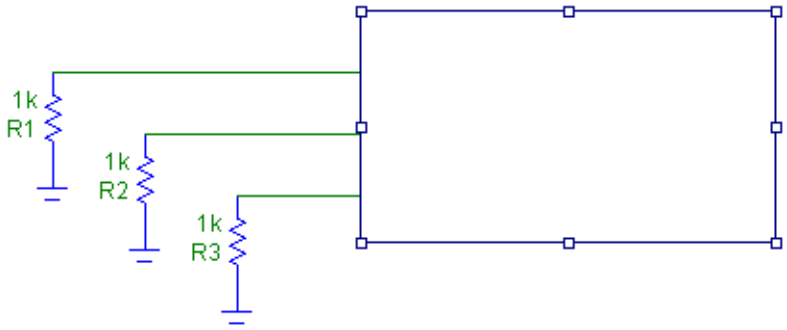


Fig. 2 - Schematic After Clear Cut Wire Operation

Creating A Schmitt Trigger Input Digital I/O Interface Model

Digital I/O models capture the electrical information common to the IC technology and circuit techniques used to design and build them. A typical digital family will only have a few I/O models. The only difference in the I/O models within a digital family is to account for the different circuits employed at the input or output such as open-collector outputs or Schmitt trigger inputs. An article in the Winter 2003 newsletter described creating the standard digital I/O model for the 74LV-A family from Texas Instruments. A second article in the Spring 2003 newsletter described how to create an open drain output digital I/O model for the same family. This article will expand on the previous articles in describing how to create a Schmitt trigger input digital I/O model for the 74LV-A family.

The Schmitt trigger input digital I/O model differs from the standard digital I/O model only in its analog to digital modeling, so the digital to analog portion of the model will be exactly the same as the standard model. This article will emphasize the differences between the two models which will be in the digital output device model statement, the AtoD interface subcircuit, and the I/O model statement. To understand the basics of the digital I/O model, read the Winter 2003 article.

Digital Output Device (O Device) Model Statement

The digital output device is the component that converts an analog voltage into its equivalent digital state for when an analog node is connected to a digital input. It does the conversion by assigning voltage ranges to the digital states. If the analog input voltage falls within a range, the output will be the corresponding digital state. These voltage ranges are defined in the model statement for the O device. The Schmitt trigger input will need only one O device model statement since it will not have any of the rise, fall, or unknown intermediate states. The O model statement for the 74LV-A Schmitt trigger input is:

```
.model DO74LV-A_ST doutput (
+  s0name="0"  s0vlo=-.5  s0vhi=2
+  s1name="1"  s1vlo=1.35   s1vhi=7)
```

The DO74LV-A_ST model simulates the hysteresis of the Schmitt trigger through the overlapping voltage ranges of the s0vhi and s1vlo parameters. The hysteresis value is determined by the difference between the two: s0vhi - s1vlo. The s0vhi parameter is defined from the VT+ positive going threshold voltage, and the s1vlo parameter is defined from the VT- negative going threshold voltage. The s0vlo and s1vhi parameters take their values from the minimum and maximum input voltage ranges, respectively.

The hysteresis occurs due to the progressive search that is deployed when determining the digital state for the input voltage. The search starts at the current state range. If the voltage is outside this range, it tries the next possible range. If it fails on the last specified range, it will wrap around to the first range again. If it fails all of the ranges, it will choose the range with the nearest voltage match. For example, if the input voltage is currently at 1V, the model will assign a 0 state to the digital input. The input voltage would then need to rise to over 2V before it leaves the voltage range defined for the 0 state. At that point, the model will assign a 1 state to the digital input. Subsequently, the input voltage would have to drop below 1.35V before it will exit the voltage range for the 1 state and return to the voltage range of the 0 state.

AtoD Interface Subcircuit

The AtoD interface subcircuit is the actual component that is placed between an analog component and a digital input internally when an analysis is entered. For the 74LV-A Schmitt trigger input, the subcircuit is as follows:

```
.subckt ATOD_LV-A_ST A D DPWR_3V DGND_3V
+  params: CAPACITANCE=0
O1 A DGND_3V DO74LV-A_ST DGTLNET=D IO_LV-A_ST
C1 A DGND_3V {CAPACITANCE+.1P}
D1 DGND_3V A D74
R1 A 1 170
C2 1 DGND_3V 1p
.ends
```

The AtoD subcircuit for the Schmitt trigger input model contains the same circuit structure as the standard model. The only differences between the Schmitt trigger and the standard subcircuits are in the name of the subcircuit and the models that are referenced within the subcircuit. Note that the O1 AtoD device references the DO74LV-A_ST model that was just created and the IO_LV-A_ST I/O model that will be created in the next section. Due to the CMOS process used to create these devices, the analog circuitry of the input is dominated by the ESD protection scheme so the Schmitt trigger input uses the same circuitry as the standard model. The 74LV-A family has no current paths to the power node in order to be able to interface directly with TTL devices, so the power node in the AtoD interface subcircuit will be left floating. The power node is still available as it is frequently used in many digital families, and it is displayed as unconnected in the schematic equivalent of the AtoD interface shown in Figure 3.

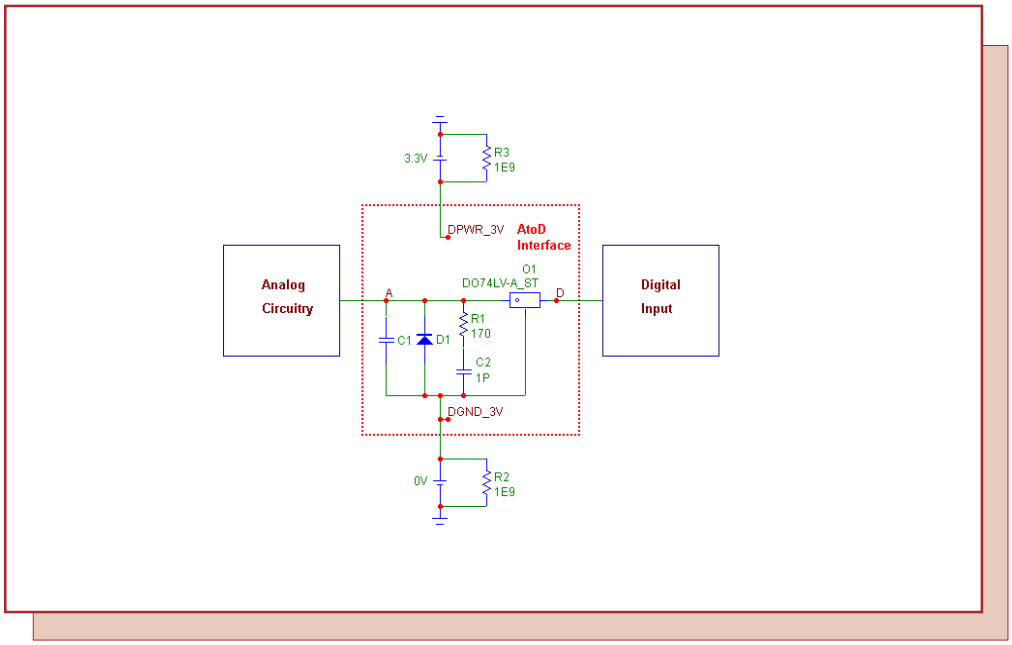


Fig. 3 - AtoD Schematic Equivalent

I/O Model Statement

The I/O model provides the information necessary to determine the output strength when devices are wire-ored together and to create the interface circuits when the digital part is connected to an analog part. The model brings together all of the interface subcircuits and models for use by a digital component. The Schmitt trigger I/O model statement for the 74LV-A family appears as follows:

```
.model IO_LV-A_ST uio (
+  DRVH=130 DRVL=130
+  INLD=2.1p
+   ATOD1="ATOD_LV-A_ST"  ATOD2="ATOD_LV-A_ST"
+   ATOD3="ATOD_LV-A_ST"  ATOD4="ATOD_LV-A_ST"
+   DTOA1="DTOA_LV-A" DTOA2="DTOA_LV-A"
+   DTOA3="DTOA_LV-A" DTOA4="DTOA_LV-A"
+   TSWHL1=2.80n  TSWHL2=2.80n
+   TSWHL3=2.80n  TSWHL4=2.80n
+   TSWLH1=2.01n  TSWLH2=2.01n
+   TSWLH3=2.01n  TSWLH4=2.01n
+  DIGPOWER="DIGIFPWR_3V")
```

The Schmitt trigger input I/O model retains many of the same values as the standard model. Most of the parameters reference the DtoA or power supply characteristics of the model and will not change.

The INLD capacitance parameter defines the input load capacitance in order to compute the optional loading delay through the device to account for excessive capacitive loading on the node caused by high fan-out. In this case, it is defined with an average input capacitance value of 2.1pF for the Schmitt trigger devices within the 74LV-A family.

The ATOD1 through ATOD4 parameters define the names of the analog to digital interface subcircuits that will be called when a digital input is connected to an analog component. These parameters have all been defined with the 'ATOD_LV-A_ST' Schmitt trigger AtoD interface subcircuit created previously. This AtoD subcircuit is applicable for all four levels, so all four parameters share the same value.

Example 74LV-A Family Digital Device

The 74LV14A inverter subcircuit below shows how the I/O model is referenced in an actual device.

```
.SUBCKT 74LV14A  1A  1Y
+     optional: DPWR_3V=$G_DPWR_3V DGND_3V=$G_DGND_3V
+     params: MNTYMXDLY=0 IO_LEVEL=0

U1 inv DPWR_3V DGND_3V
+     1A 1Y
+     DLY_LV14 IO_LV-A_ST MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}

.model DLY_LV14 ugate (tplhTY=9.6ns tplhMX=16.3ns tphlTY=9.6ns tphlMX=16.3ns)

.ENDS  74LV14A
```

Note that the inverter device within the subcircuit uses IO_LV-A_ST as its I/O model name. The 74LV14A inverter is tested in the circuit configuration shown in Figure 4. A 3.3V triangle wave is placed at the input of the inverter. The resistor lets Micro-Cap plot the output as an analog voltage. The simulation of the circuit in Figure 5 shows the hysteresis capability of the model.

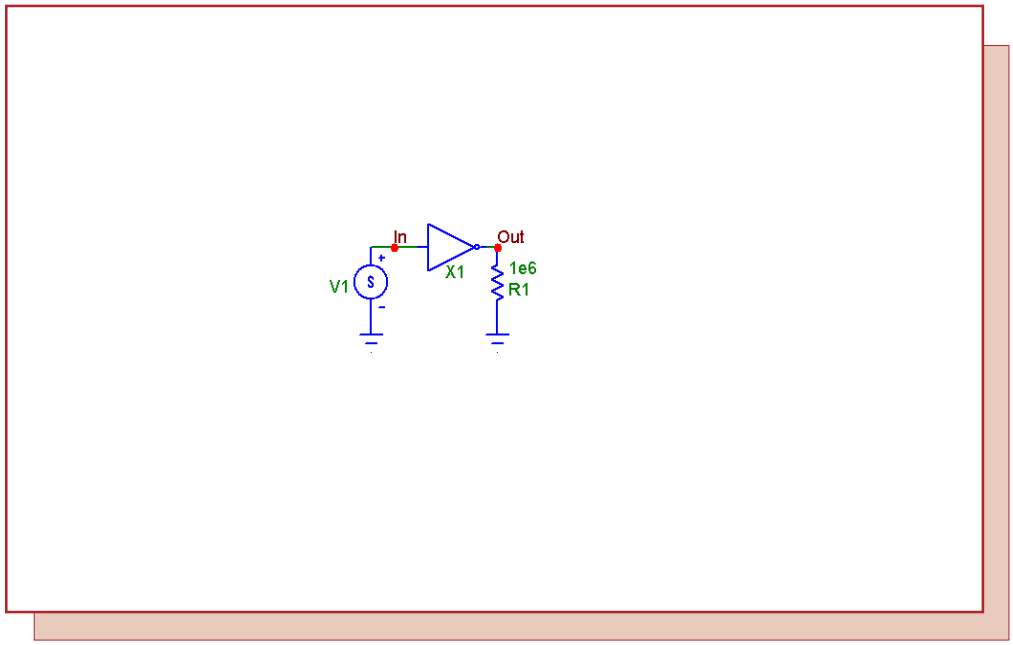


Fig. 4 - 74LV14A Test Circuit

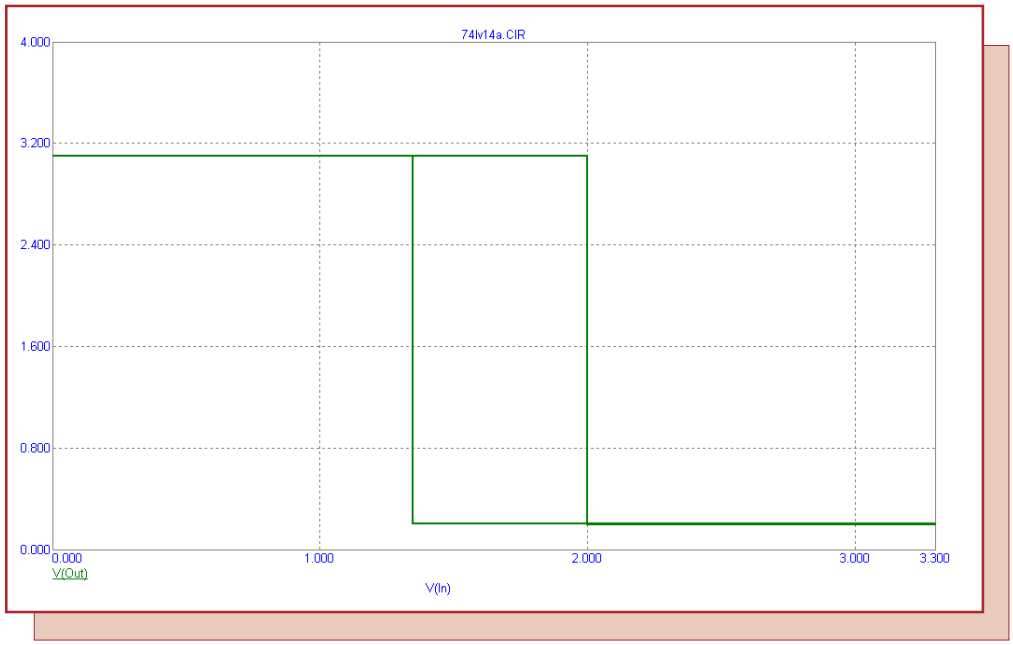


Fig. 5 - 74LV14A Test Analysis

Smooth Transition Time Switch

The Switch component in Micro-Cap has a time dependent method that defines a time window during which the switch can be on or off. The transition times between the on and off resistance values of the switch are instantaneous. These instantaneous transitions can occasionally cause problems with simulation convergence depending on the configuration of the circuit such as when a switch is in series with an inductor. One method to improve the convergence is to create a time switch equivalent using the S (V-Switch) component in conjunction with a nonlinear function voltage source. An example of this equivalent switch is used in Figure 6.

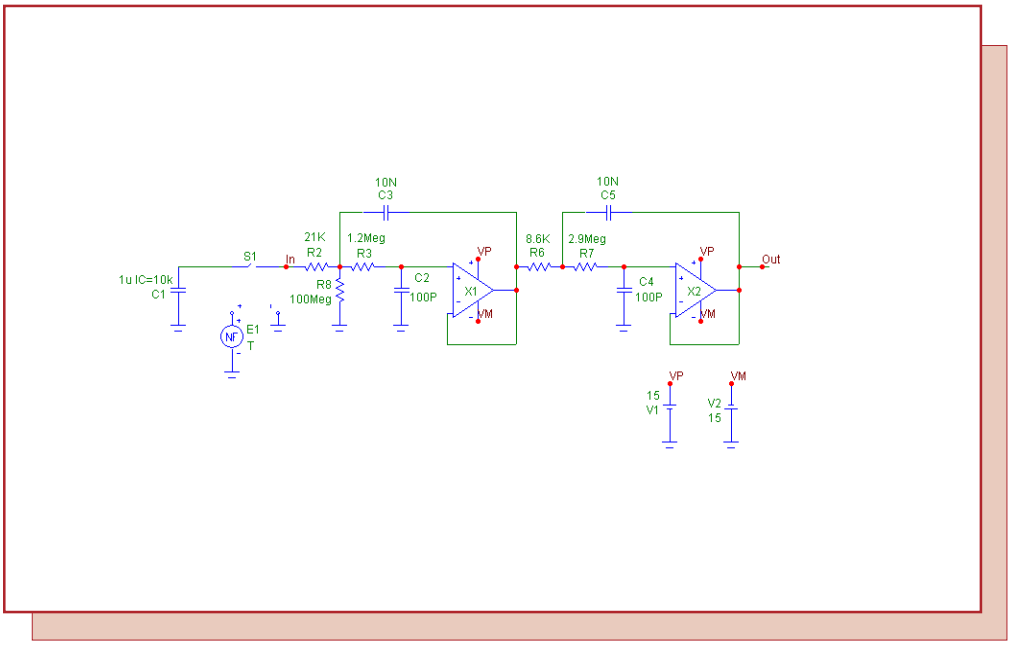


Fig. 6 - Smooth Transition Time Switch Circuit

The smooth transition time switch is modeled through the S1 and E1 components in the schematic. The S1 component is a S (V-Switch) voltage switch. The MODEL attribute is defined as TIME1 with a corresponding model statement in the text area of:

.MODEL TIME1 VSWITCH (ROFF=1G RON=1m VON=1m VOFF=.95m)

When the input voltage to the switch is less than .95mV, the switch will be off and at a resistance of 1G. When the input voltage source is greater than 1mV, the switch will be on and at a resistance of 1m. Between .95mV and 1mV, the resistance is transitioning between its off and on values. In this range, the switch uses an exponential function to detemine its resistance. This function provides a smooth resistive transition between the on and off values which provides a more robust convergence technique. The E1 source is an NFV function source that has its VALUE attribute defined as T. During transient analysis, this source will produce a voltage that is equivalent to the current time being simulated. Since the E1 source is used as the voltage input to the switch, the combination of the two components mimic a time switch.

In this schematic, the input of the circuit is a 1uF capacitor that has been initially charged with 10kV across it. The switch is used in series with the capacitor to simulate a 10kV pulse. At 1ms, the switch has been turned on to let the voltage pass through to the low-pass Butterworth filter that follows it. The resulting step response analysis is displayed in Figure 7. The two waveforms plotted are the input and output of the low-pass filter.

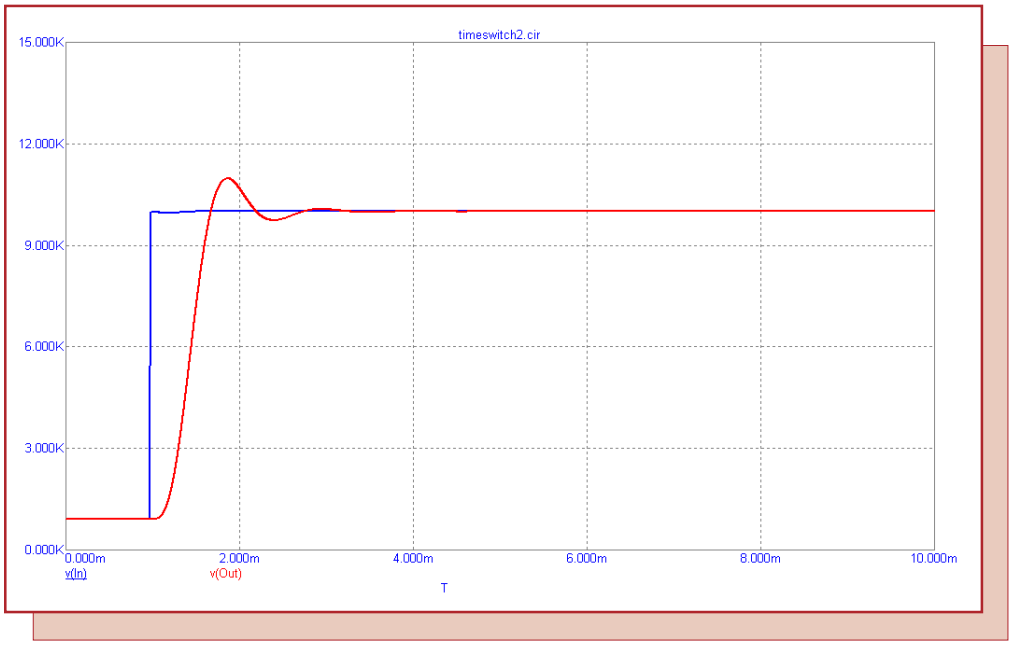


Fig. 7 - Time Switch Analysis

A nice feature of the Switch component is that it is easy to create a window of time where the switch may be defined as either on or off. The S (V-Switch) and NFV component combination only models one of these transitions. In order to create a switch that can produce the equivalent of the time window, two S (V-Switch) components must be used. The schematic in Figure 8 shows the two possible orientations that can be created to model the time window equivalent. The top circuit has two of the switches in series that use the two following model statements:

.MODEL TIME1 VSWITCH (ROFF=1G RON=1m VON=1m VOFF=.95m)
.MODEL TIME2 VSWITCH (ROFF=1G RON=1m VON=5m VOFF=5.05m)

Both switches must be on for the voltage to pass through them. The combination of the two switches produces a time window between 1ms and 5ms where the equivalent switch will be on. Below .95ms and above 5.05ms, one of the two switches will be off, so the equivalent switch will be off during those times. The bottom circuit has two of the switches in parallel that use the two following model statements:

.MODEL TIME3 VSWITCH (ROFF=1G RON=1m VON=.95m VOFF=1m)
.MODEL TIME4 VSWITCH (ROFF=1G RON=1m VON=5m VOFF=4.95m)

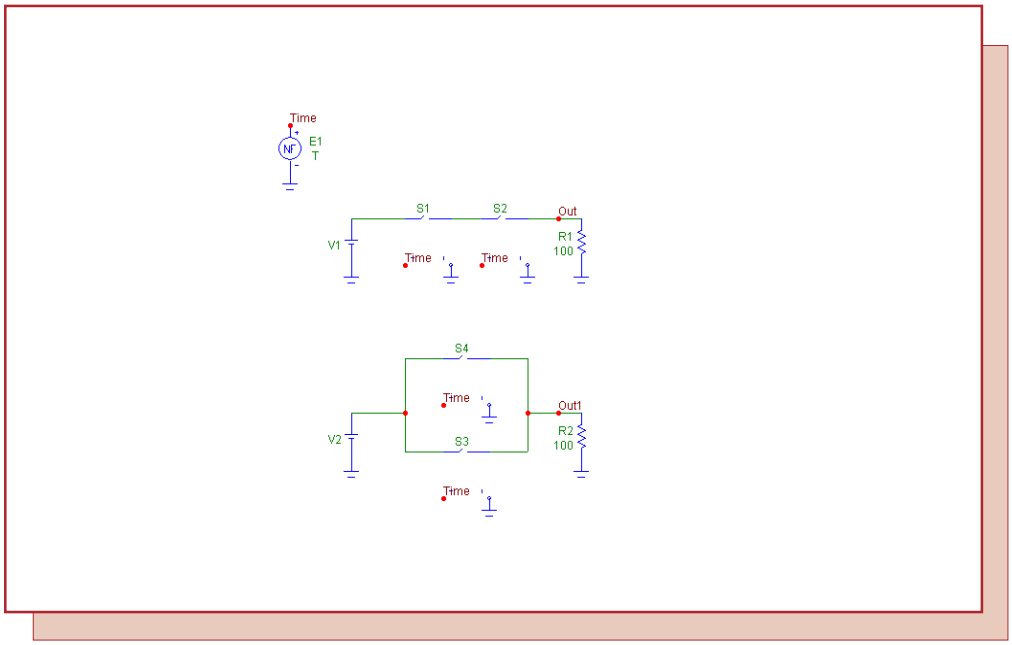


Fig. 8 - Time Window Switch Equivalent

Either of the switches can be on in order to let the voltage pass through them. The combination of these two switches produces a time window between 1ms and 5ms where the equivalent switch will be off. Below .95ms and above 5ms, one of the two switches will be on, so the equivalent switch will be on during those times.

The input to all four of these switches is the E1 source at the top which has been defined as T to represent the simulation time. Only one source is needed for any number of the S (V-Switch) components since the time input to all the switches is an independent variable.

Each of these configurations has a 10V battery at its input and is followed by a 100 ohm resistive load. The analysis of these two configurations is displayed in Figure 9. The top plot is the waveform at the resistive load for the series combination of switches. The battery voltage has been passed through to the resistor between 1ms and 5ms where the time window equivalent switch has been defined as on.

The bottom plot is the waveform at the resistive load for the parallel combination of switches. Note that the voltage is now zero during the time window between 1ms and 5ms since that is the time range that has been modeled as the off state.

This technique provides a good way of overcoming convergence problems when a time switch is present in a schematic and should be one of the first methods used in trying to overcome any convergence errors that occur during a time switch transition.

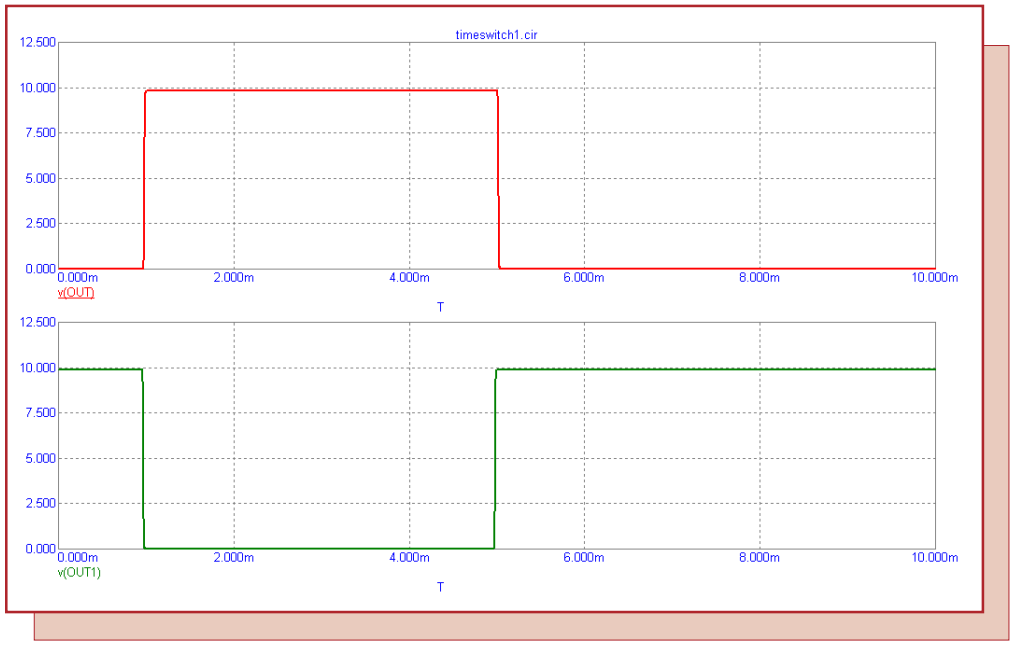


Fig. 9 - Time Window Switch Analysis

Diode Materials Temperature Parameter Values

When modeling a diode at the nominal temperature of 27C, the actual material of the diode is irrelevant. As long as the diode parameters that have been defined for the model can appropriately simulate the current and capacitance curves, the resulting model will be applicable to the simulation. If the simulation is running at a temperature other than 27C, then the EG and XTI diode temperature parameters must be defined with respect to the semiconductor material of the diode being modeled.

The EG parameter defines the energy gap of the diode in electronvolts. This parameter is completely dependent on the semiconductor material being used in creating the diode. The XTI parameter defines the temperature exponent for the IS current. At 27C, neither of these parameters will have an effect. At other temperatures, the EG and XTI parameters should be defined according to the semiconductor material as shown below:

Material	EG	XTI
Silicon	1.11	3
Schottky	.69	2
Germanium	.67	3
GaAs	1.43	3
GaP	2.26	3

To demonstrate the effect that these two temperature parameters have on a diode, the schematic in Figure 10 has been created in order to produce the basic If-Vf curve of the diode. The top circuit consists of a battery that will drive the D1 diode that is in series with it. The battery voltage in the schematic has been set to 5V, but that will be overwritten when the DC sweep is performed. The bottom circuit has an NFV source that duplicates the battery voltage in order to drive a second diode, D2. The only difference between the two diode models is that the D2 diode has had its T_ABS parameter set to 27. This diode will always run at 27C no matter what the temperature defined in the analysis limits is. This will provide us a baseline If-Vf curve to compare to.

To produce the desired If-Vf curve, a DC analysis is run. In the DC Analysis Limits dialog box, the V1 battery is swept from 0V to 1V in .001V increments. A linear step method is chosen for this example. The temperature field has been set to 50C so that the temperature parameters will influence the results. Both the EG and the XTI parameters of the D1 diode are set up to be stepped. The EG parameter is stepped through the list '1.11,.69,.67,1.43,2.26' and the XTI parameter is stepped through the list '3,2,3,3,3'. These two parameters are stepped simultaneously so that there will be five curves in the analysis with each curve simulating one of the materials shown in the table above.

The resulting If-Vf curves are displayed in Figure 11. The red waveform displays the If-Vf curve of the diode when it is running at 27C. At this temperature, the semiconductor material doesn't have an effect. The other five curves simulate the If-Vf curve at a temperature of 50C for each of the semiconductor materials that are in the table. Each curve is labelled with the semiconductor material that it represents. The germanium and Schottky curves are nearly on top of each other since the EG parameters each uses are nearly equivalent. As expected, the GaP semiconductor material shows the greatest divergence from the nominal curve due to it having the largest energy gap. The default temperature parameters for the diode model are set to model silicon.

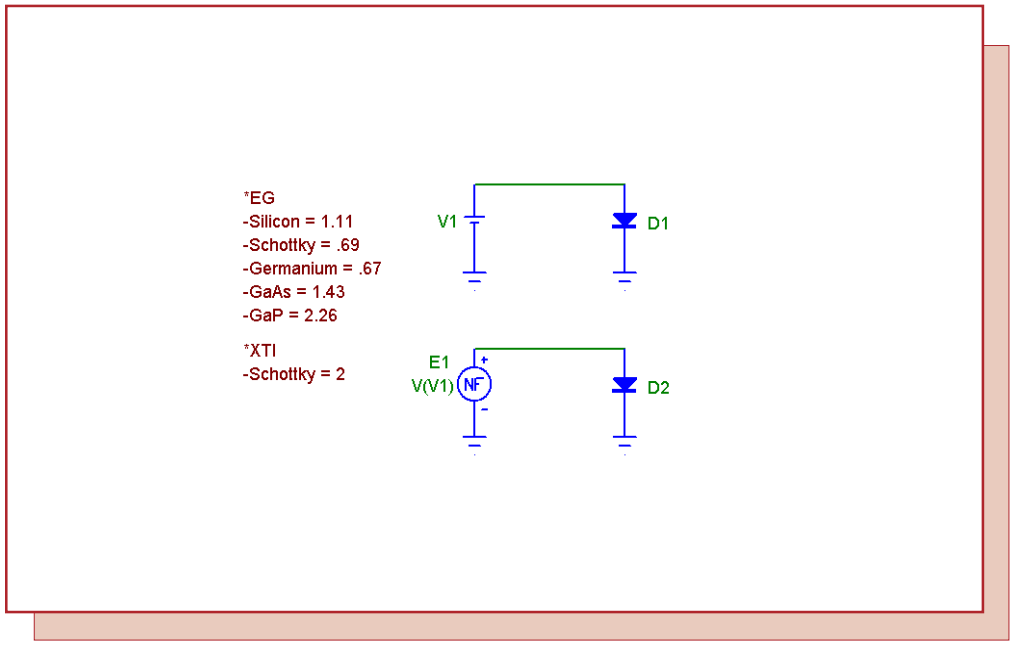


Fig. 10 - Diode I-V Schematic

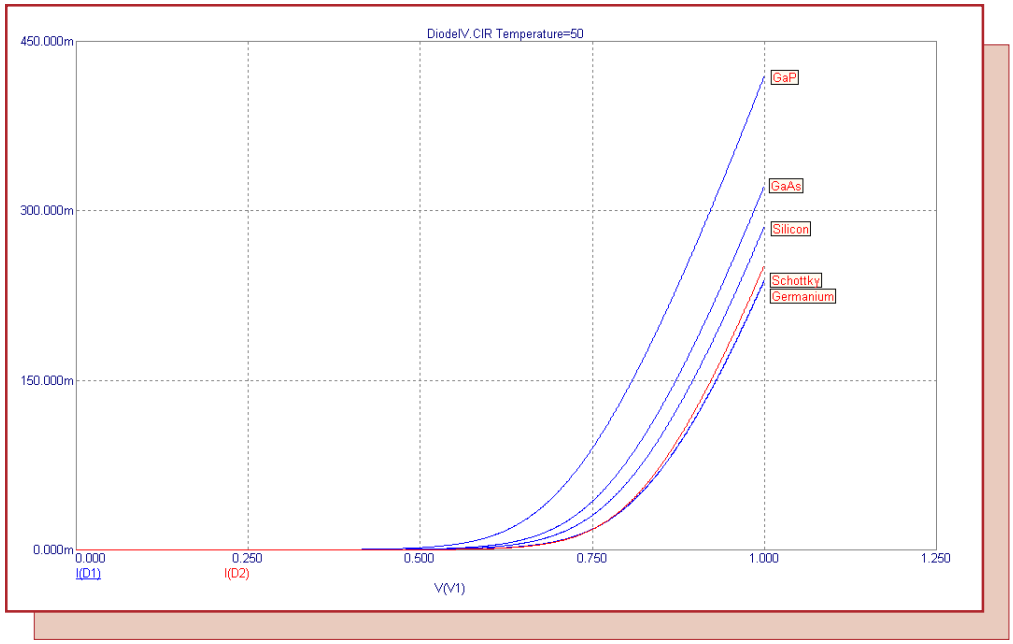


Fig. 11 - Stepping Eg and Xti Diode Parameters

Product Sheet

Latest Version numbers

Micro-Cap 7 ..... Version 7.2.2
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