

Applications for Micro-Cap[™] Users

Spring 2003 News



User Source Files

Featuring:

- Creating An Open Drain Output Digital I/O Interface Model
- Creating And Using User Source Files
- Optimizing AC Analysis Frequency Step Sampling

News In Preview

This newsletter's Q and A section describes how to bypass an initial transient and what defines the beta curve of a transistor. The Easily Overlooked Features section describes the navigation buttons that are available within the Attribute dialog box.

The first article describes the process of creating an open drain digital I/O interface model for the 74LV-A family.

The second article is a tutorial on how to create and use User Source files.

The third article describes how to optimize the frequency step sampling during an AC analysis simulation.

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Book Recommendations

General SPICE

- Computer-Aided Circuit Analysis Using SPICE, Walter Banzhaf, Prentice Hall 1989. ISBN# 0-13-162579-9
- *Macromodeling with SPICE*, Connelly and Choi, Prentice Hall 1992. ISBN# 0-13-544941-3
- Inside SPICE-Overcoming the Obstacles of Circuit Simulation, Ron Kielkowski, McGraw-Hill, First Edition, 1993. ISBN# 0-07-911525-X
- The SPICE Book, Andrei Vladimirescu, John Wiley & Sons, Inc., First Edition, 1994. ISBN# 0-471-60926-9

MOSFET Modeling

• MOSFET Models for SPICE Simulation, William Liu, Including BSIM3v3 and BSIM4, Wiley-Interscience, First Edition, ISBN# 0-471-39697-4

VLSI Design

• Introduction to VLSI Circuits and Systems, John P. Uyemura, John Wiley & Sons Inc, First Edition, 2002 ISBN# 0-471-12704-3

Micro-Cap - German

• Schaltungen erfolgreich simulieren mit Micro-Cap V, Walter Gunther, Franzis', First Edition, 1997. ISBN# 3-7723-4662-6

Micro-Cap - Finnish

• *Elektroniikkasimulaattori*, Timo Haiko, Werner Soderstrom Osakeyhtio, 2002. ISBN# ISBN 951-0-25672-2

Design

- Microelectronic CircuitsHigh Performance Audio Power Amplifiers, Ben Duncan, Newnes, First Edition, 1996. ISBN# 0-7506-2629-1
- Microelectronic Circuits., Adel Sedra, Kenneth Smith, Fourth Edition, Oxford, 1998

High Power Electronics

- Power Electronics, Mohan, Undeland, Robbins, Second Edition, 1995. ISBN# 0-471-58408-8
- Modern Power Electronics, Trzynadlowski, 1998. ISBN# 0-471-15303-6

Switched-Mode Power Supply Simulation

• SMPS Simulation with SPICE 3, Steven M. Sandler, McGraw Hill, First Edition, 1997. ISBN# 0-07-913227-8

• Switch-Mode Power Supply SPICE Simulation Cookbook, Christophe Basso, McGraw-Hill 2001. This book describes many of the SMPS models supplied with Micro-Cap.





Micro-Cap Questions and Answers

Question: I am running transient analysis on my circuit. There is an initial transient start-up in the simulation that I'm not interested in. I would like to start the simulation at the steady state point. Is there a way to bypass the initial transient?

Answer: The initial transient would have to be simulated. However, once the transient is complete, you can save the data at that point of the simulation and use it to initialize another simulation run. The operation for that is as follows:

1) Set the time range in the Transient Analysis Limits to the time at which you want to save the data.

2) Run the simulation.

3) Go to the Transient menu and choose State Variables Editor.

4) Click on the Write command button and save the file name as circuitname.top where

circuitname is the name of your circuit. Close the State Variables Editor.

5) Go to the Transient menu and choose Limits.

6) In the limits dialog box, disable the Operating Point option if it is on and change the State Variables option to Read.

7) Set the time range to the length you want to simulate and run the simulation.

Question: I'm using a 2N4265 NPN BJT in my circuit. The circuit seems to run fine, but I was looking at the model parameters for this BJT and the BF is specified at 1.13172K. That seems way too high in comparison to the data sheet values of hFE. What am I missing here?

Answer: In SPICE, many of the parameters in the model statement are curve fitting parameters. These often don't have a direct correlation to the data sheet values. For a BJT, the Beta vs Ic curve is actually calculated using four parameters: BF, NE, ISE, and IKF. The ISE and NE parameters model the additional base current that reduces the beta at low base-emitter voltages. The IKF parameter models the high-current reduction in beta.

To see the actual beta curve in Micro-Cap, use the Plot feature in the Attribute dialog box. Choose to plot the DC Current Gain and it will display the beta curve for that transistor model.

Easily Overlooked Features

This section is designed to highlight one or two features per issue that may be overlooked because they are not made visually obvious with a toolbar button.

Navigate Buttons in the Attribute Dialog Box

The navigate buttons scroll through the parts that are present in the schematic. They are a means to quickly navigate to another component in the schematic without having to close the Attribute dialog box. The navigate buttons are found in the bottom right corner of the Attribute dialog box as shown in Figure 1.

Battery X
Value Value Value Value Value Value Value Value
Display Pin Markers Pin Names Pin Numbers V Current V Power V Condition
PART=V3 Voltage vs. Time
VALOE=BY SLIDER_MIN=0 SLIDER_MAX=6 PACKAGE= COST= POWER=
OK Cancel Font Add Delete Help
New Syntax Plot Expand Help Bar Browse

Fig. 1 - Attribute Dialog Box

The navigate buttons function as follows:

These buttons navigate to another part of the same part type. For example, if the current part in the Attribute dialog box is a resistor, then clicking one of these buttons will take you to another resistor in the schematic. The order of the parts is determined by when they were placed in the schematic.

These buttons navigate to another part of a different part type. For example, if the current part in the Attribute dialog box is a battery, then clicking one of these buttons may take you to a resistor or a pulse source. The type that is navigated to depends on what is in the schematic, and what the current part type is.

The component that is displayed in the Attribute dialog box will be highlighted in the schematic in the background.

Creating An Open Drain Output Digital I/O Interface Model

Digital I/O models capture the electrical information common to the IC technology and circuit techniques used to design and build them. A typical digital family will only have a few I/O models. The only difference in the I/O models within a digital family is to account for the different circuits employed at the input or output such as open-collector outputs or Schmitt-trigger inputs. An article in the Winter 2003 newsletter described creating the standard digital I/O model for the 74LV-A family from Texas Instruments. This article will expand on the previous article in describing how to create an open drain output digital I/O model for the 74LV-A family.

The open drain output digital I/O model differs from the standard digital I/O model only in its digital to analog modeling, so the analog to digital portion of the model will be exactly the same as the standard model. This article will emphasize the differences between the two models which will be in the digital input device model statement, the DtoA interface subcircuit, and the I/O model statement. To understand the basics of the digital I/O model, read the Winter 2003 article.

Digital Input Device (N Device) Model Statement

The digital input device is the device within the interface that converts a digital output node to its analog equivalent. It does the conversion by translating the digital states to impedance changes on the analog side. Two resistors (RLO and RHI) are placed in a voltage divider configuration between the power and ground nodes of the digital device. These resistors determine the equivalent analog voltage of the digital output. The model statement for the N device defines the values of the resistors for each digital state, and the switching time between the old resistance and the new resistance when a state change occurs. The model statement for the open drain output N device in the 74LV-A family is:

```
.model DIN74LV-A_OD dinput (
```

```
+ s0name="0" s0tsw=3.4n s0rlo=31.9 s0rhi=494.5 ;@30ohms, .2V
+ s1name="1" s1tsw=3.4n s1rlo=1Meg s1rhi=1Meg
+ s2name="F" s2tsw=3.4n s2rlo=58.1 s2rhi=73.2 ;@32.4 ohms, 1.46V
+ s3name="R" s3tsw=3.4n s3rlo=58.1 s3rhi=73.2 ;@32.4 ohms, 1.46V
+ s4name="X" s4tsw=3.4n s4rlo=58.1 s4rhi=73.2 ;@32.4 ohms, 1.46V
+ s5name="Z" s5tsw=3.4n s5rlo=1Meg s5rhi=1Meg)
```

Since the open drain output only affects the 1 and Z states of a digital component, the 0, F, R, and X states will retain the same values as they had in the standard model. The 1 state has its RHI and RLO resistances defined arbitrarily with values of 1Meg. The resistance values are defined with a high value in order to minimize their impact on the pullup resistor that is typically attached to the output of an open drain device. The Z, high impedance, state is already defined with high resistance values, but the switching time should be set to the same switching time as is defined for the 1 state. For the 74LV-A family, the switching times were already the same so no change is needed.

DtoA Interface Subcircuit

The DtoA interface subcircuit is the actual component that is placed between a digital output and an analog component internally when an analysis is entered. For the open drain output model, the subcircuit is as follows: .subckt DTOA_LV-A_OD D A DPWR_3V DGND_3V + params: CAPACITANCE=0 DRVH=0 DRVL=0 N1 A DGND_3V DPWR_3V DIN74LV-A_OD DGTLNET=D IO_LV-A_OD CLOAD A DGND_3V {CAPACITANCE+.1p} .ends

The DtoA subcircuit for the open drain model contains the same circuit structure as the standard model by having only an N (digital input) device and a load capacitor. The only differences between the open drain and the standard subcircuits are in the name of the subcircuit and the models that are referenced within the subcircuit. Note that the N1 DtoA device references the DIN74LV-A_OD model that was just created and the IO_LV-A_OD I/O model that will be created in the next section. There is no need to model the high impedance element of the open drain output explicitly in this subcircuit since it is specified in the N device model statement for both the 1 and Z states. The schematic equivalent of the DtoA subcircuit interface appears in Figure 2.



Fig. 2 - Open Drain DtoA Schematic Equivalent

I/O Model Statement

The I/O model provides the information necessary to determine the output strength when devices are wire-ored together and to create the interface circuits when the digital part is connected to an analog part. The model brings together all of the interface subcircuits and models for use by a digital component. The I/O model statement for the 74LV-A open drain output appears as follows:





.model IO_LV-A_OD uio (

- + DRVH=1Meg DRVL=130
- + INLD=2.3p
- + ATOD1="ATOD_LV-A" ATOD2="ATOD_LV-A_NX"
- + ATOD3="ATOD_LV-A" ATOD4="ATOD_LV-A_NX"
- + DTOA1="DTOA_LV-A_OD" DTOA2="DTOA_LV-A_OD"
- + DTOA3="DTOA_LV-A_OD" DTOA4="DTOA_LV-A_OD"
- + TSWHL1=3.42n TSWHL2=3.42n
- + TSWHL3=3.42n TSWHL4=3.42n
- + TSWLH1=0.16n TSWLH2=0.16n
- + TSWLH3=0.16n TSWLH4=0.16n
- + DIGPOWER="DIGIFPWR_3V")

The open drain output I/O model retains some of the same values as the standard model. The DRVL, INLD, ATOD1, ATOD2, ATOD3, ATOD4, and DIGPOWER parameters will all have the same values. Most of these define the input characteristics or the power supply for the device which do not change. The DRVL parameter stays the same since the open drain output will only affect the high state output of the device.

The DRVH parameter is arbitrarily assigned the value of 1Meg. This parameter defines the high state output strength that is used to resolve the output state when multiple digital outputs are wire-ored together. With an open drain output, the drive strength is weak and so is defined with a high resistance value. The open drain output devices are typically dependent on pullup resistors to provide the drive resistance.

The DTOA1 through DTOA4 parameters define the names of the digital to analog interface subcircuits that will be called when a digital output is connected to an analog component. These parameters have all been defined with the 'DTOA_LV-A_OD' open drain DtoA interface subcircuit created previously. This DtoA subcircuit is applicable for all four levels, so all four parameters share the same value.

The TSWLH1 through TSWLH4 and TSWHL1 through TSWHL4 define the switching times for the I/O model. The switching times are subtracted from the digital device's propagation delay on outputs which are connected to analog components so that the analog signal at the other side of the DtoA interface should reach the switching level just when the digital device does at the stated delay. Since the same DtoA subcircuit is used for all four cases in this family, the switching times will be the same for each level of a transition.

The switching time parameters in the I/O model are initially set to 0. To measure the switching times, a schematic similar to the one in Figure 3 may be used. The schematic consists of two separate circuits. The only difference between the two circuits is that the top one has a minimal load capacitance of .1pF and a 1K pullup resistor whereas the bottom circuit has no load at all. The 1K pullup resistor value in the top circuit was taken from the waveform test circuits in the 74LV05A data sheet. The two digital stimulus sources start in the zero state, at 100ns transition to the one state, and at 200ns transition back to the zero state. These sources are fed into 74LV05A inverters which reference the IO_LV-A_OD I/O model. A transient analysis is run on this schematic with the results displayed in Figure 4. Three waveforms are plotted: D(In), D(OutD), and V(OutA). D(In) is the digital input waveform from one of the stimulus sources. D(OutD) is the digital output waveform of the inverter with no load. Note that for the D(OutD) waveform, its high state is actually represented with a Z (high impedance state). This occurs due





Fig. 3 - Switching Time Measurement Circuit



Fig. 4 - Switching Time Measurement Analysis



to the high DRVH value in the I/O model, and the fact that there is no pullup resistor on the output to drive the node to a 1 state. V(OutA) is the output voltage waveform of the inverter with an analog load. The switching time is measured from the point that the no-load output makes its transition to when the analog load output reaches either the Vih or Vil value depending on the transition. For example, to measure the high to low switching time, one cursor is placed at the point where the D(OutD) waveform has a ZL transition, and the other cursor is placed at the point where the analog output reaches its Vil voltage which in this case is .8V. The switching time is the time differential between these two points which comes out to 3.42ns for the open drain model. Similarly, for the low to high switching time, one cursor is placed at the LZ transition for D(OutD), and the other cursor is placed at the point where the analog output reaches at the point where the analog output reaches two points which comes out to 3.42ns for the open drain model. Similarly, for the low to high switching time, one cursor is placed at the LZ transition for D(OutD), and the other cursor is placed at the point where the analog output reaches its Vih voltage which is 2V for this model. The low to high switching time is measured at 0.16n. The switching time parameters are then updated with these new values.

Example 74LV-A Open Drain Output Device

The 74LV05A inverter from the switching time measurement shows how the I/O model is referenced in an actual device.

.SUBCKT 74LV05A 1A 1Y

- + optional: DPWR_3V=\$G_DPWR_3V DGND_3V=\$G_DGND_3V
- + params: MNTYMXDLY=0 IO_LEVEL=0

U1 inv DPWR_3V DGND_3V

- + 1A 1Y
- + DLY_LV05 IO_LV-A_OD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}

.model DLY_LV05 ugate (tplhTY=4.7ns tplhMX=10.6ns tphlTY=5.8ns tphlMX=10.6ns)

.ENDS 74LV05A

Note that the inverter device within the subcircuit uses IO_LV-A_OD as its I/O model name.

Creating And Using User Source Files

The user source file provides a powerful method for importing analysis waveforms contained within a file. There are two main uses for a user source file in Micro-Cap. The first is to use the file with a user source to create an input voltage in a schematic. Unorthodox waveforms that can't be easily represented with standard Micro-Cap sources such as the sine or pulse source can be imported with this method. The second use is to replot the waveform during another analysis run using the CurveX or CurveY operators. Replots can be used in order to compare waveforms from different runs or even different schematics.

Creating A User Source File

Since the user source file is an ASCII text file, a file can be created through any text editor just by implementing the correct header and data format. The header can be created simply by copying and pasting from one of the existing .USR files available in the DATA directory and making a few basic edits for the number of data points and the waveform names. A previous newsletter article in the Fall 2002 issue described the process of converting an Excel file into a user source file and details the format needed to manually create a user source file. For this article, we will cover the most common method of creating such a file by using the Save Curves options in the Analysis Properties dialog box.

To be able to access the Save Curves option, a simulation must first be run. The Save Curves option in the Properties dialog box is available in transient, AC, and DC analysis only after a simulation has been performed. The Save Curves page appears in Figure 5. The simulation used as an example in this case is the transient analysis of the AD16.CIR file that is distributed with Micro-Cap. The AD16 circuit takes an input NFV source and funnels it through 16 bit AtoD and DtoA components to produce a sampled analog waveform at the output. The waveform we are interested in saving is the output of the DtoA component which would be quite a laborious task to reproduce in another schematic using the standard sources.



Fig. 5 - Save Curves Page in the Analysis Properties Dialog Box





On the left hand side of the Save Curves page is a list of all of the available waveforms that may be saved to a user source file. Simply select the waveform that is to be saved to the file. If there are any stepping or Monte Carlo runs in the analysis, drop down lists will appear at the top of the page that let one specific waveform be chosen out of the family of runs. The As (New Name) field lets the user specify the name that the waveform is to be assigned to within the user source file. This name will be used when the waveform is imported through a User Source or through the CurveX and CurveY operators. The In File field specifies the name and location of the file that the waveform information will be stored in. Multiple waveforms may be stored in one file. The Save button will save the waveform to the specified file. If a waveform already exists with the same name in the specified file, it will be overwritten. The Delete button lets any waveform that already exists in the specified file be deleted.

For the AD16.CIR example, highlight the V(Out) waveform in the Curves list. For the name and file, the default values will be used as follows:

Name: V(Out) vs T File: AD16.USR

Finally, click the Save button, and the V(Out) waveform will be saved to the AD16.USR file.

Importing As A Voltage Source Input

The User Source, which is available in the Analog Primitives/Waveform Sources section of the Component menu, provides the capability to import waveforms from the user source file and use them as voltage sources in a schematic. The schematic in Figure 6 displays an example circuit with a User Source as the input. The User Source voltage is being fed into a delay Bessel filter that has a 0dB gain and a delay of 5ns. To import the waveform that was saved from the AD16 circuit, the User Source has its attributes defined as:

FILE: AD16.USR EXPRESSION: V(Out) vs T

The FILE and EXPRESSION attributes have been defined to match the entries from the Save Curves page. Clicking the drop down arrow next to the Value field, when the FILE or EXPRESSION attribute is selected, displays a choice of available files or waveforms within a specified file, respectively. The resulting transient analysis is displayed in Figure 7. Note that the voltage at node In is the output voltage waveform from the AD16 circuit.

Importing As A Plotted Waveform

A user source waveform can also be plotted directly in the analysis through the use of the CurveX and CurveY operators. For the AD16 waveform, setting the Y Expression in the Transient Analysis Limits dialog box to:

CurveY("AD16","V(Out) vs T")

will import the waveform directly into the analysis. A simple technique to define the Curve operator is to do a right mouse click in the Y Expression field, which will invoke an expressions menu. One of the topics in the menu is Curve which provides a listing of all available user source file waveforms in the current data directory.



Fig. 6 - User Source Example Circuit



Fig. 7 - User Source Analysis



Optimizing AC Analysis Frequency Step Sampling

AC analysis is a linear, small signal analysis. This means that all circuit variables are assumed to be linearly related. Due to the linearity, there is not an internal data step control such as can occur in transient analysis when increased data sampling is needed. For some AC runs, particularly simulations involving narrow band operation, the frequency step sampling can have a significant impact on the final plot results. The frequency step sampling is controlled by combinations of the Frequency Step option, the Number of Points field, and the Maximum Change % field in the AC Analysis Limits dialog box as follows:

Frequency Step is Auto: This method uses the first plot of the first group as a pilot plot. If, from one frequency point to another, the plot has a vertical change greater than the Maximum Change % of the Y scale, the frequency step is reduced, otherwise it is increased.

Frequency Step is Linear: This method produces a frequency step such that, with a linear X scale, the data points are equidistant horizontally. The Number of Points field determines the total number of data points that will be calculated.

Frequency Step is Log: This method produces a frequency step such that with a log X scale, the data points are equidistant horizontally. The Number of Points field determines the total number of data points that will be calculated.

Frequency Step is List: This method calculates data points only at the frequencies specified in the commadelimited list within the Frequency Range field. There is no frequency step.

The Number of Points field will also be available if numeric output is enabled for any waveform, but if the Frequency Step is set to Auto, it will just interpolate data points in the numeric output, not force more data points to be calculated. Only when the Frequency Step is set to Linear or Log is the Number of Points field used to determine the number of data points calculated.

The default Frequency Step is set to Auto since this normally produces the best simulations for any frequency range. However, some AC analysis simulations need a greater number of data points to be adequately sampled than the default settings produce. Narrow band circuits in particular must have data sampled through the narrow band range of frequencies to produce a complete analysis. The schematic in Figure 8 is one such circuit. This schematic has a 1A AC current source at its input. In series with this source is a 100 ohm resistor which is then connected to a two branch parallel resonant network.

The desired output in AC analysis for this circuit is to measure the impedance of the resonant frequency. Since the I1 current source has been defined as a 1A source, the voltage at node Out will be equivalent to the resonant network impedance. The impedance for the circuit has a very narrow resonant peak that occurs at 10kHz. Figure 9 shows the AC simulation when the frequency step is Auto and the Maximum Change % is 5 which are both the default settings in Micro-Cap. The expected resonant peak is not apparent in the simulation. The View Data Points option for the simulation has been enabled. As can be seen in the figure, very few data points are being calculated in this run. The resonant frequency has been bracketed with one data point at 7.3kHz and the next data point at 13.7kHz so the entire resonant area is being skipped over. The area between the data points is just straight line interpolation. Since the simulation is flat at the start of the run, it easily falls within the 5% Maximum Change % versus the Y axis. Each time it meets this criteria, the frequency step is





Fig. 8 - AC Sampling Example Circuit

increased. By the point of the resonant frequency, the frequency step is large enough that it never samples in that area. The actual data points that are being calculated are perfectly correct. The problem is that not enough data points are being calculated.

One solution to increase the number of data points is to use the Log frequency step and to increase the Number of Points value. The Log step is chosen over the Linear step in this case because the frequency range of the simulation spans a couple of decades, and the X Axis is set to a log scale. The Number of Points field is set to 10001 to ensure a fine sampling during the analysis. The subsequent simulation is displayed in Figure 10. Note the dramatic increase in the number of data points that have been calculated versus the original simulation. The resonant frequency is now very obvious.

While the Log frequency step and the Number of Points field were used in this case, making the Maximum Change % smaller in conjunction with the Auto frequency step would also have increased the accuracy. Setting the Maximum Change % to .1 would have created a comparable simulation. The Log and Linear frequency steps do have the advantage of producing a consistent data sample throughout the entire frequency range.

There is no one frequency step combination that will be correct for every simulation. Much depends on the frequency range that the circuit is being simulated across and the type of operation the circuit performs. Enabling the Data Points in the View section under the Scope menu gives a good idea of the frequency sampling that is being performed and makes it easy to determine if the number of data points needs to be increased.







Fig. 9 - Frequency Step = Auto



Fig. 10 - Frequency Step = Log

Product Sheet

Latest Version numbers

Micro-Cap 7	Version	7.2.0
Micro-Cap 6	Version	6.3.3
Micro-Cap V	Version	2.1.2

Spectrum's numbers

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