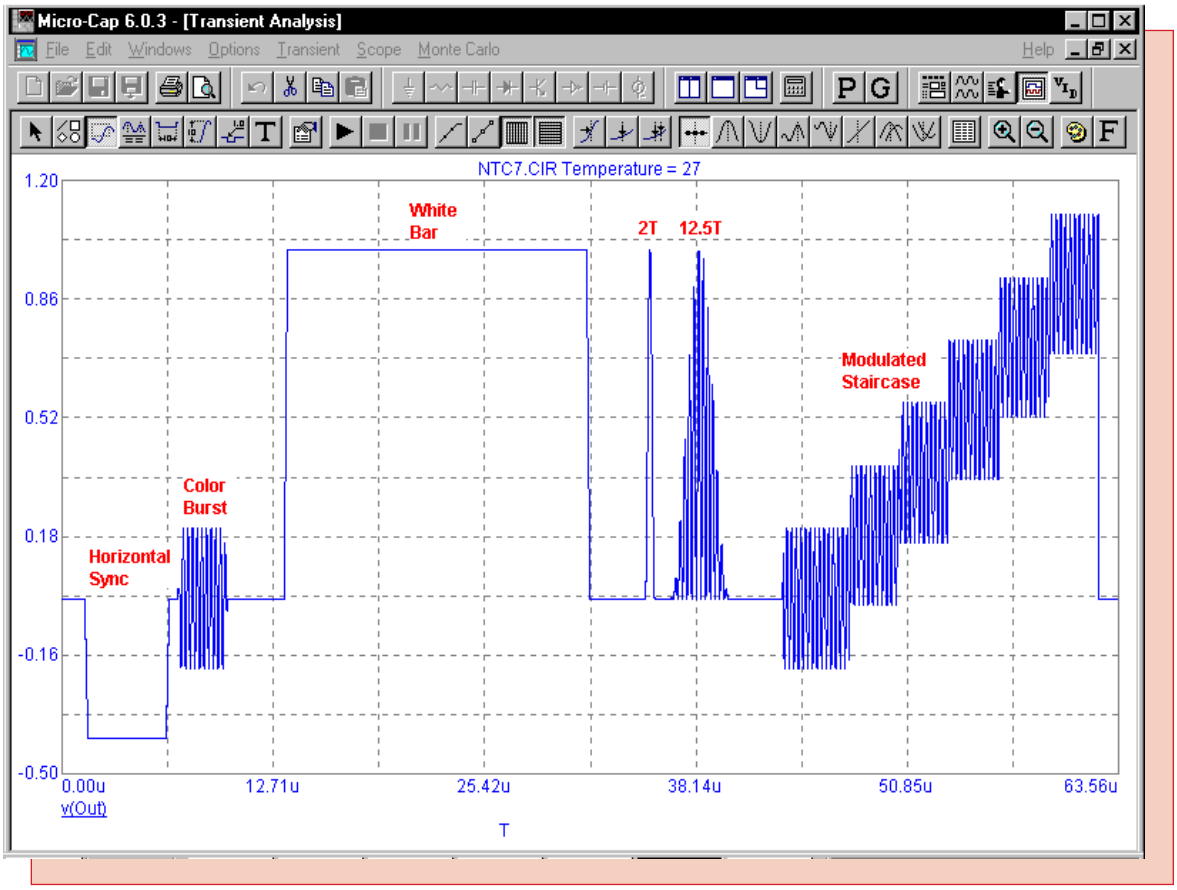
spectrum news

Applications for Micro-Cap™ Users

Fall 1999

NTC7 Test Signal



Featuring:

- Merging Components and Shapes into Micro-Cap 6
- Using Global Nodes
- Monte Carlo Error Reports
- NTC7 Test Signal

News In Preview

This issue is the first newsletter issue to use Micro-Cap 6 for its applications. The first article describes how to merge component and shape files from a previous or current version of Micro-Cap into new files in order to keep the user's components and shapes separate from the standard files that are distributed with Micro-Cap. The next article describes how to use the global node capability that is present in Micro-Cap 6, which lets you connect nodes on different levels of the schematic by using a common node name. The third article describes how to use the Monte Carlo error reporting capability and how to generate a schematic from any errors that were reported. The last article describes the creation of a NTC7 composite test signal for video systems by using multiple sources available in Micro-Cap.

Contents

Book Recommendations

Micro-Cap / SPICE

- *Computer-Aided Circuit Analysis Using SPICE*, Walter Banzhaf, Prentice Hall 1989. ISBN# 0-13-162579-9
- *Macromodeling with SPICE*, Connelly and Choi, Prentice Hall 1992. ISBN# 0-13-544941-3
- *Semiconductor Device Modeling with SPICE*, Paolo Antognetti and Giuseppe Massobrio McGraw-Hill, Second Edition, 1993. ISBN# 0-07-002107-4
- *Inside SPICE-Overcoming the Obstacles of Circuit Simulation*, Ron Kielkowski, McGraw-Hill, First Edition, 1993. ISBN# 0-07-911525-X
- *The SPICE Book,* Andrei Vladimirescu, John Wiley & Sons, Inc., First Edition, 1994. ISBN# 0-471-60926-9
- *SMPS Simulation with SPICE 3,* Steven M. Sandler, McGraw Hill, First Edition, 1997. ISBN# 0-07-913227-8
- *MOSFET Modeling with SPICE Principles and Practice,* Daniel Foty, Prentice Hall, First Edition, 1997. ISBN# 0-13-227935-5

German

- *Schaltungen erfolgreich simulieren mit Micro-Cap V,* Walter Gunther, Franzis', First Edition, 1997. ISBN# 3-7723-4662-6

Design

- *High Performance Audio Power Amplifiers,* Ben Duncan, Newnes, First Edition, 1996. ISBN# 0-7506-2629-1

Micro-Cap 6 Question and Answer

Question: I have a SPICE text file from another program that I want to analyze in Micro-Cap. The name of the file is RINGDIF.CIR. Whenever I try to load this in Micro-Cap, I get an error stating that I "Must run CONVERT for 'RINGDIF.CIR' to force a conversion." Is it possible to analyze a SPICE text file?

Answer: Both SPICE and PSpice text files can be run directly in Micro-Cap. The problem in this case is the extension of the file RINGDIF.CIR. Micro-Cap assumes that any file with the extension .CIR is a schematic file, and since it doesn't recognize the SPICE file as a compatible schematic format, it returns the convert error. The procedure for fixing this is simple. Just change the extension of the file to .CKT. The file RINGDIF.CKT would be able to load and run without a problem.

Question: I have created a circuit that contains an opamp. The opamp is only being used for its gain capability so I have no need for all of the other modelling capabilities of it such as slew rate limiting, saturation, offset, etc. How can I change the opamp model so it is an ideal opamp?

Answer: Double click on the opamp while in select mode to invoke its Attribute dialog box. In this dialog box, highlight the MODEL= attribute by clicking on that line in the list window. When this attribute is highlighted, the Edit command button in the bottom right of the dialog box should be enabled. Click on the Edit button. This extends the dialog box in order to display the parameters of the model statement. Changing the Level parameter to a value of 1 will model an ideal opamp. The only parameters that are used with the Level 1 opamp are the A, ROUTAC, and ROUTDC. This model level is represented by a current source and a resistor.

Question: I am running a Probe Transient Analysis on my circuit. When the analysis is finished, the schematic portion of the split screen has some of its wires missing. I can click on where the wire should be and a waveform will appear, and when I exit analysis and go back to the schematic, the wires are fine again. What is happening?

Answer: The wires that are disappearing should be connected to a node that is purely digital. (Purely digital nodes can be known from the fact that when the node numbers are displayed, the node number is within a rectangle. For analog and mixed nodes, the node number is within an oval.) In a Probe analysis or when in Animation mode for an analysis, the wires connected to digital nodes will change color to represent the last digital state that has been calculated at that node. In the case described, the color of the wire for the state calculated happens to match the background color of the window making it appear as if the wire disappeared.

To view the defined colors of the digital states, invoke the Properties dialog box for the schematic. This dialog box can be invoked by hitting the F10 hotkey, double clicking in the schematic while in select mode, or by clicking on the Properties icon. Go to the Color/Font page of the dialog box. At the bottom of the Objects list are the digital state entries. Highlight an entry to view or edit its color.

Easily Overlooked Features

This section is designed to highlight one or two features per issue that may be overlooked because they are not made visually obvious with an icon or a menu item.

Navigating Schematics
There are multiple methods for navigating schematics. The best method to use depends both on the individual user and the size of the schematic. The first two methods are common to any Windows user.

Schematic scrolling
Scroll the schematic using the vertical or horizontal scroll bars. This is the conventional method.

Scaling
Use the Zoom-Out or Zoom-In commands to be able to resize the schematic with a different zoom scale to get your bearing.

The next few methods are often easier to use but not as obvious as the first two.

Panning
Pan the schematic. Panning means to move the view to a different part of the schematic. In keyboard panning, you use CTRL+<CURSOR KEY> to move the view in the direction of the cursor key arrow. This movement is similar to using the mouse on the scroll bars. A simpler method and what many consider the best method to navigate over smaller distances of a schematic is mouse panning. In mouse panning, you click and hold the right mouse button while dragging the mouse. The effect is like sliding a piece of paper across a desktop in the direction of the mouse movement.

Centering
Centering uses the SHIFT+right click method to navigate. While holding down the SHIFT button, click the right mouse button at the point that you want centered in the window. Clicking toggles the scale between 1:1 and 1:4 and centers the schematic at the mouse position. A useful situation for this method is when you have a large schematic that you are working on at a 1:1 scale. A single SHIFT+right click will shrink the schematic to a 1:4 scale. You can then visually scan the schematic to see the part of the schematic that you would like to work on next. Another SHIFT+right click on that part of the schematic will center it in the window at a 1:1 scale.

Flagging
Place flags at locations you expect to revisit in the schematic through the Flag mode. Enter Flag mode, and then click in the schematic. A text dialog box will appear that lets you define the name of the flag. Once a flag is placed, clicking on the flag icon in the lower right window corner will display a list of all of the flags that are in the schematic. Choosing one of the flags from the list will center the schematic window on that flag. This method has the bonus of working between different pages of the schematic.

Merging Components and Shapes into Micro-Cap 6

Micro-Cap 6 is the first generation of Micro-Cap simulators to let the user have access to multiple component and shape files simultaneously. This setup has obvious benefits. One of the main benefits is that the user can now place any of his own macros, subcircuits, or other new components into a file separate from the main Micro-Cap file. If Micro-Cap is upgraded or reinstalled, these files are not in danger of being overwritten. For a new user, simply open up a new Shape file in the Shape Editor and Component file in the Component Editor, and add the new parts into those files. For a user who is upgrading from MC4 or MC5, the procedure for merging the components from a previous version into a new file in MC6 is as follows.

The Shape Editor

In the Shape Editor, the only thing to do is to set up a new file that the shapes can be copied into when a merge operation is performed. Perform the following steps:

1) Go to the Windows menu and choose Shape Editor.
2) In the Shape Editor, click on the New File icon, and a new file will be created with just a Blank shape.
3) Click on the Save File icon to rename the file. A .SHP extension must be used.
4) Make sure that the shape file that you want to merge into is the one currently selected from the list of files. This means that the Shape Editor is currently displaying the list of shapes from that file. The shape file selected when the Shape Editor is closed will be the shape file that any shapes that need to be merged will be sent to.
5) Close the Shape Editor and save it when prompted.

The actual merge operation is performed in the Component Editor.

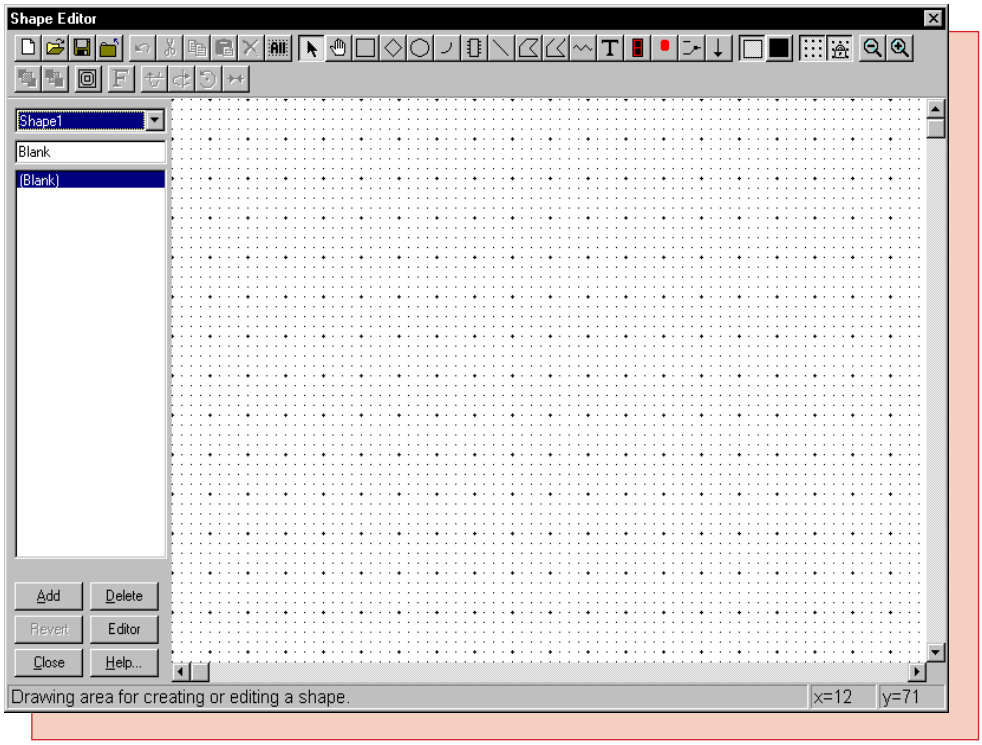


Fig. 1 - New File in the Shape Editor

Component Editor
The Component Editor is the editor that has the merge capability within it. To merge from a previous version of Micro-Cap to a new file within MC6, perform the following steps.

1) Go to the Windows menu and choose Component Editor.
2) In the Component Editor, click on the New File icon, and a new file will be created that contains a single empty group.
3) Highlight the file name which will appear similar to 'C:\mc6\new.cmp'. The name of the component file can then be edited in the File text field at the top of the screen. The extension of the file must be .CMP.
4) Click on the Merge icon.
5) In the Open Component dialog box, select the file that is to be merged into the highlighted file. Any MC4, MC5, or MC6 component files may be merged. Select the appropriate type in the Files of type field. Once the file is selected, hit Open. This begins the process of merging. The merge operation will compare the file to be merged with the files in the Component Editor. Any component whose name does not currently exist in the Component Editor will be merged into the selected file. When the merge operation finds a component that does not exist in the currently loaded files, it will check to see if that component's shape exists in the Shape Editor files. If that shape does not exist, it will copy the shape over into the last selected shape file. If the file to be merged is from MC5 or MC6, the components will be placed in the new file in the same group as they existed in the old one. When merging to a new file, it is then possible to have groups of the same name in each of the files in the Component Editor. To edit a group name, simply highlight it and edit the name in the Group text field.
6) Close the Component Editor and save it when prompted.

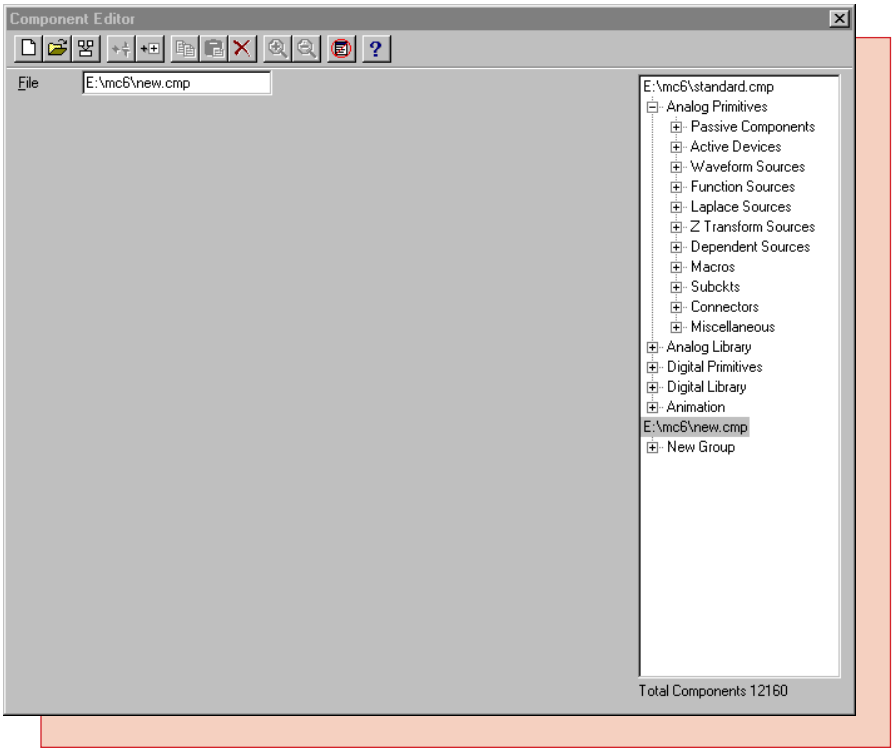


Fig. 2 - New File in the Component Editor

The merge only brings over the component's schematic information. Any macro circuit or library would have to be copied over by the user. Remember that in the case of libraries, you may need to add the library name into the NOM.LIB file which resides in the DATA subdirectory of MC6. Open up the NOM.LIB file in Micro-Cap or in any text editor. On a new line, type in the following:

.lib "mylib.lib"

where mylib.lib represents the name of the library file. This statement also assumes that the library is in the same path as the NOM.LIB file. If the library is kept in a directory other than the one that the NOM.LIB is present in, a path would have to be added into the .lib reference, such as:

.lib "c:\project1\mylib.lib"

Once these procedures are finished, an MC4 or MC5 circuit that uses one of the user's components can be loaded and run in MC6.

Using Global Nodes

In a schematic, it is a common occurrence for multiple components to share the same power supply. When all of the power supply pins are on the main level, it is easy to wire the pins together or label each pin with the same node name which will connect them together without wiring. If the schematic is a multiple level schematic, it is easier to use a global node to connect the power supply pins rather than trying to wire them together. Micro-Cap has the capability to define any node as a global node which will make it accessible by all subcircuits or macros without having to be passed as a parameter argument. A global node is defined by giving the node a name in the following format:

$G_name

The $G_ at the beginning of the node name signifies to Micro-Cap that this node is to be treated as a global node. For a schematic, entering a node name is done by going into Text mode, and then clicking on the node. When the text dialog box comes up, type in the node name and hit OK. When a piece of text is used as a node name, a pin connection will be placed on the node where the bottom left corner of the text touches the node. For a subcircuit, simply edit the node name in the text file so that it has the above format.

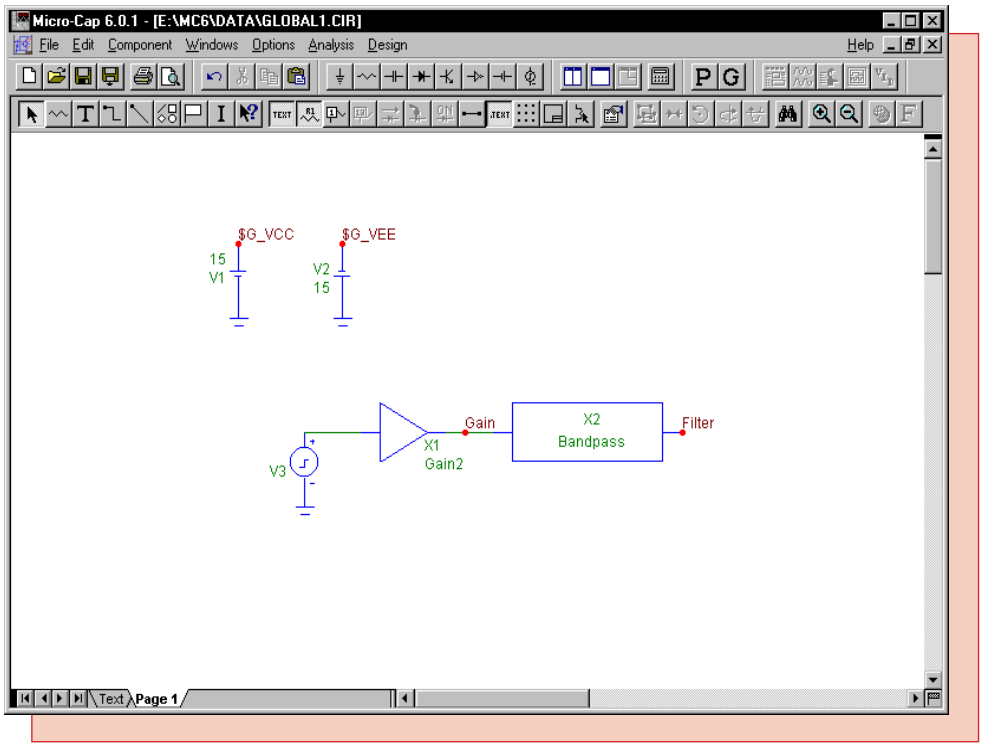


Fig. 3 - Global Nodes Sample Circuit

The schematic in Figure 3 gives an example of the use of global nodes. The circuit consists of a pulse source that is input to a gain macro whose output goes into a bandpass filter subcircuit. As seen in the figure, neither the gain stage nor the bandpass filter stage have any external power pins. In the upper left of the schematic are two batteries. These two batteries have their non-ground nodes labelled as $G_VCC and $G_VEE. Due to the global naming of the nodes, the two voltages of the batteries are accessible in any level of the schematic.

The schematic in Figure 4 is the macro circuit for the gain macro. The circuit contains an opamp in the standard inverting gain of two configuration. The key to this macro is that the positive and negative supply pins on the opamp component have been labelled using the global node names, $G_VCC and $G_VEE. Since the power supplies are global, the nodes PinA and PinB are the only nodes that need to be passed to the main circuit.

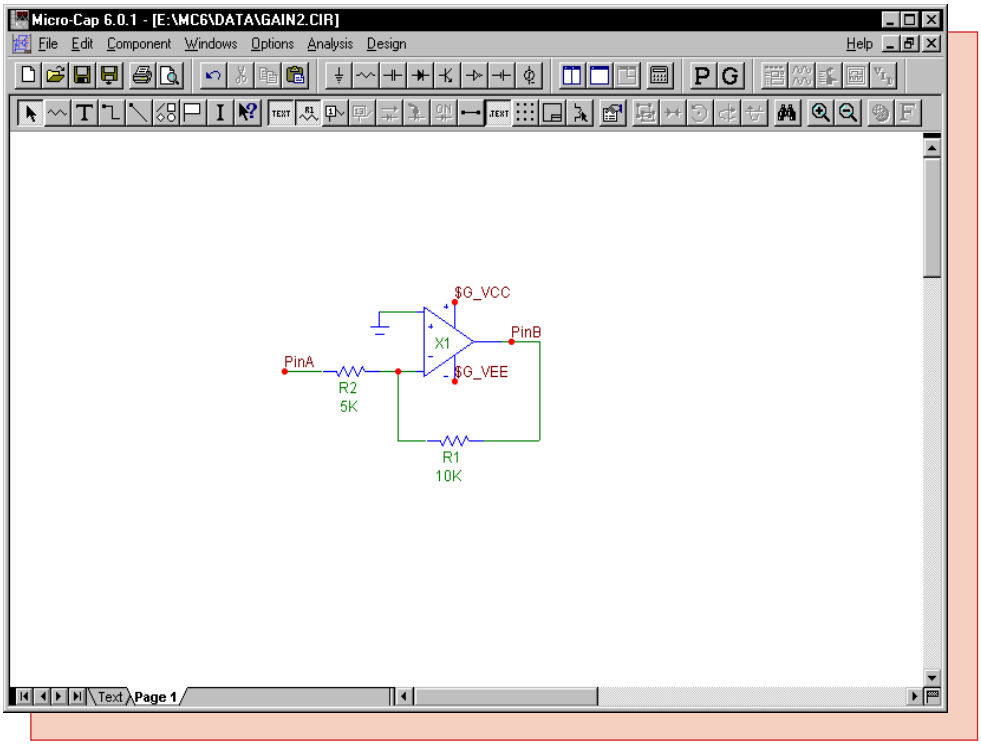


Fig. 4 - Macro Using Global Nodes

The bandpass filter subcircuit models a Butterworth bandpass filter with a gain of 0dB. It has a 20dB stopband attenuation with a center frequency of 1KHz, a passband of 100Hz, and a stopband of 400Hz. This filter was created through the Active Filter Designer in Micro-Cap, and then converted to a SPICE listing with the Translate to SPICE file option. The subcircuit consists of the following listing:

```
.SUBCKT   BANDPASS   IN   OUT
C1   0   1   CM1   10.02506N
C2   1   3   CM1   10.02506N
C3   0   8   CM1   10.02506N
C4   8   9   CM1   10.02506N
R1   1   In   RM1   641.46204K
R2   0   3   RM1   23.29013K
R3   0   4   RM1   31.32138K
R4   6   4   RM1   90.83004K
R5   1   6   RM1   23.29013K
R6   0   1   RM1   24.1676K
R7   8   6   RM1   597.59976K
R8   0   9   RM1   21.69758K
R9   0   10   RM1   29.17967K
```

```
R10  Out  10  RM1  84.61921K
R11  8  Out  RM1  21.69758K
R12  0  8  RM1  22.51505K
X1  3  4  $G_VEE  6  $G_VCC  UA747C
X2  9  10  $G_VEE  Out  $G_VCC  UA747C
*
.MODEL  RM1  RES  (R=1  LOT=1%)
.MODEL  CM1  CAP  (C=1  LOT=1%)
.ENDS
*  OPAMP
*  PINS:   1=NC+  2=NC-  3=VEE  4=VO  5=VCC
.SUBCKT  UA747C  1  2  3  4  5
C1  6  7  8.66025e-012
C2  12  13  3e-011
CE  10  14  1e-019
D1  18  19  D
D2  20  18  D
D3  4  16  D
D4  17  4  D
D5  3  5  D
E1  14  0  POLY(2)  5  0  3  0      0  0.5  0.5
F1  13  14  POLY(5)  VS1  VC  VE  VLP  VLN  0  4.24413e+007  -4.24413e+007
+   4.24413e+007   4.24413e+007   -4.24413e+007
GA  12  0  6  7      0.000188496
GCM  0  12  10  0      5.96075e-009
H1  18  0  VS2  1000
IEE  10  3  1.516e-005
Q1  6  2  8  QINN
Q2  7  1  9  QINP
R2  12  11  100000
RC1  5  6  5305.16
RC2  5  7  5305.16
RE1  8  10  1837.31
RE2  9  10  1837.31
RE  10  14  1.31926e+007
RO2  13  14  25
ROUTAC  15  4  50
RP  5  3  18165.2
VC  5  16  1
VE  17  3  1
VLN  0  20  25
VLP  19  0  25
VS1  11  0  0
VS2  13  15  0
*
.MODEL  D  D  ()
.MODEL  QINN  NPN  (BF=83.3333)
.MODEL  QINP  NPN  (BF=107.143  IS=1e-016)
.ENDS  UA747C
```

Listing 1 - Bandpass Filter Subcircuit

The bandpass filter subcircuit calls a second subcircuit, the UA747C opamp, within it. The calls to the UA747C subcircuit are the lines that start with X1 and X2. Two of the nodes in each of these calls are defined as the global nodes, $G_VCC and $G_VEE. These nodes in the call correspond to the positive and negative power supply pins from the opamp subcircuit.

Due to the labelling of the global nodes, the batteries in the main circuit provide the power for the opamp in the gain macro circuit, and the two opamps that are called within the bandpass subcircuit. One very nice result of this is that the power supply for the entire circuit is easily changed by simply editing the batteries on the main circuit.

The AC analysis simulation of the main circuit appears in Figure 5. The circuit has been simulated from 0Hz to 2KHz. Two waveforms have been plotted. These waveforms are the gain in dB at the output of the gain macro, and the gain in dB at the output of the filter. The gain from the gain macro is a constant 6.02dB over this frequency range as can be expected from an amplifier with a gain of 2. The gain from the filter shows the bandpass characteristics of the filter at the 1KHz center frequency.

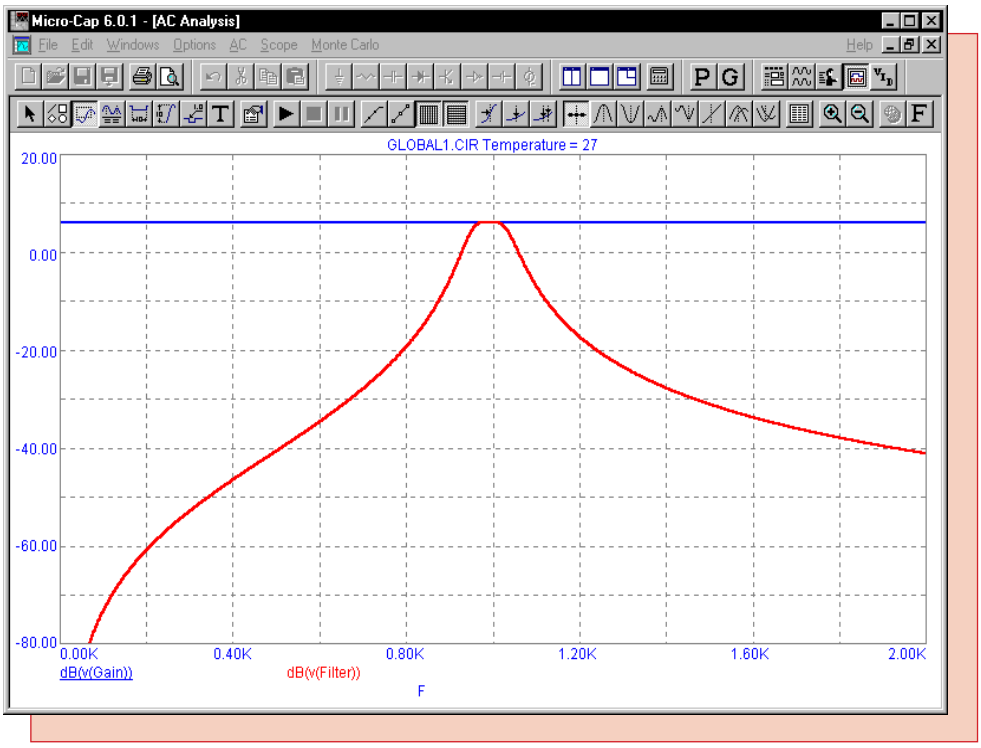


Fig. 5 - Analysis of Global Nodes Circuit

Monte Carlo Error Reports

Monte Carlo analysis provides a means of viewing how the circuit performance can be affected by parameter variation. The analysis performs a specified number of simulation runs varying the circuit randomly within the tolerances defined in the schematic. This is in order to ensure that the circuit will behave within acceptable limits while accounting for the possible variation in component values within the tolerance band. When setting up the Monte Carlo analysis options, it is possible to set an error limit that will report in the numeric output when the circuit violates the performance criteria. Micro-Cap also has the capability to convert the error report into a schematic using the component values that cause the error.

The circuit in Figure 6 is a simple RLC circuit. The pulse source input is a 5V pulse with a pulse width of 400ns and a repetition period of 1us. The pulse is in series with a 1uH inductor which then feeds to a parallel RC where the capacitor is at 1nF and the resistor is at 50 ohms. Only two of the components are toleranced in this circuit. The inductor and capacitor have been given the model names IND1 and CAP2, respectively. These models are defined in the text area as:

.MODEL IND1 IND (L=1.0 LOT=10%)
.MODEL CAP2 CAP (C=1.0 LOT=10%)

The L and C parameters are merely multipliers. For example, the L parameter will multiply its value by the number defined in the VALUE attribute of the inductor. The result of this product will be the inductance value of the inductor. Since the L and C parameters are both defined as 1, placing a 10% tolerance on these parameters will tolerance the final inductance and capacitance by 10%.

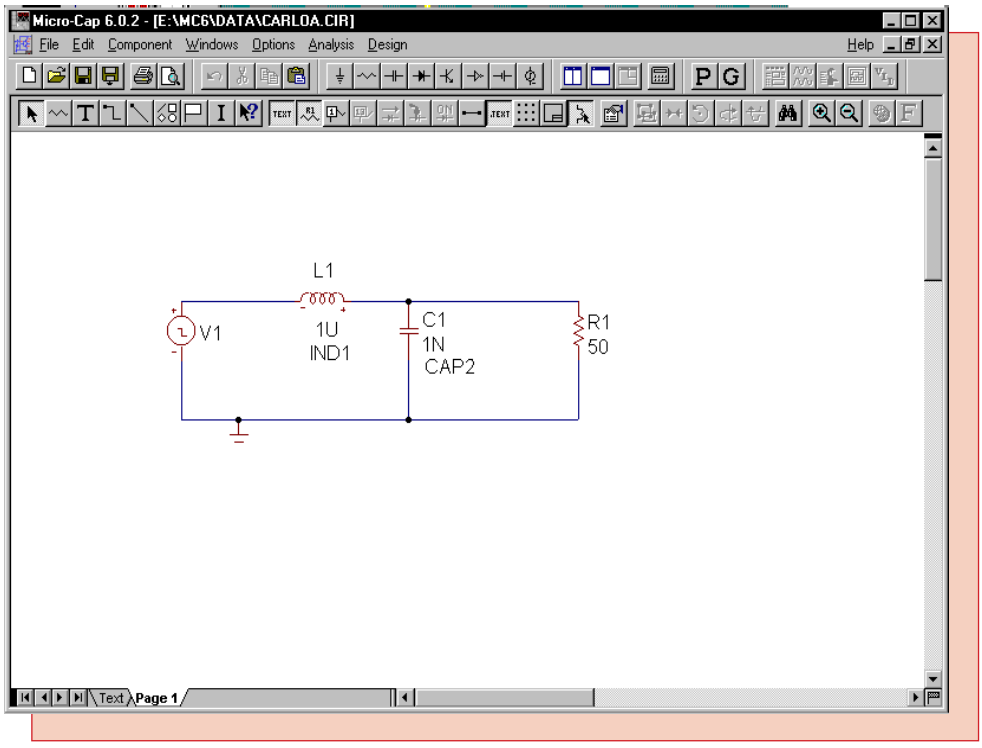


Fig. 6 - Monte Carlo Schematic

In each of the analyses, there is a Monte Carlo menu available on the main window. When first entering the analysis, you can either close the Analysis Limits dialog box or click on the window in the background to access the Monte Carlo menu. The Options choice under this menu lets you set up the parameters for the Monte Carlo analysis and invokes the Monte Carlo Options dialog box.

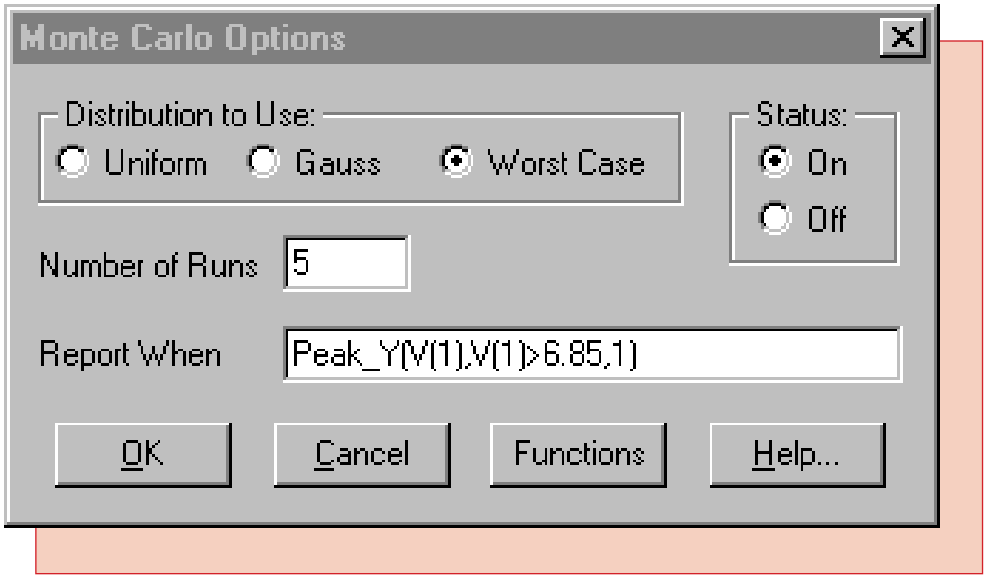


Fig. 7 - Monte Carlo Options Dialog Box

The Monte Carlo Options dialog box that appears in Figure 7 displays the settings used for this circuit in transient analysis. As can be seen in the figure, the settings show that the Monte Carlo analysis will use the worst case distribution. Since only two components are being toleranced, there are only four possible simulation runs with a worst case distribution. For this reason, the Number of Runs field has been set to five. Five was chosen rather than four because even the worst case tolerances are still chosen randomly. It is very possible that duplicate tolerance settings will be chosen before all four individual tolerance settings have been chosen. Five runs gives a greater chance for all four separate runs to appear.

The portion of the dialog box that produces the error report is the expression within the Report When text field. Micro-Cap will produce an error report whenever the expression in this field evaluates to a true condition. The expression must consist of at least one of the performance functions that exist within Micro-Cap. All of the performance functions along with their syntax can be chosen by clicking on the Functions command button. In this case, the Report When text field has been defined with the following statement:

Peak_Y(V(1),V(1)>6.85,1)

This expression uses the Peak_Y function which determines the specified Y magnitude of the nth peak in the waveform. In this case, the function is operating on the first peak of the V(1) waveform. It will evaluate to a true condition whenever the first peak of the waveform V(1) exceeds 6.85V.

Figure 8 displays the Monte Carlo transient analysis results of the circuit. Both the input and the output have been plotted.

Once the analysis is complete, opening the numeric output window of the analysis lets you view the Monte Carlo error report. Figure 9 displays the error report for the current circuit. Whenever the Report When field returns a true value, the tolerances that generate the violation are used to calculate the equivalent model statements in the numeric output. As can be seen in Figure 9, the Case 1 waveform violates the peak magnitude of 6.85V set in the Report When field. In this case, the settings that cause the error occur when the capacitor multiplier C has been toleranced to 1.1 and the inductor multiplier L has been toleranced to .9.

Once the error report is in the numeric output, Micro-Cap has the capability to generate a schematic from this report. Under the File menu, there is a Load MC File command. For each error listed in the numeric output, Micro-Cap will generate a schematic that uses the model parameters that caused the error. Note that this command may produce a lot of schematic files if there are many errors in the numeric output. This lets you simulate and edit the circuit that actually causes the error. Figure 10 shows the schematic that was generated from the error in Case 1 of the numeric output. The model names for the inductor and capacitor have each been edited to append a _1 to the end of them. In the text area, the following has been added:

Temperature = 27 Case= 1
Peak_Y(V(1),V(1)>6.85,1) occurred for the following parameters:
.MODEL CAP2_1 CAP (C=1.1)
.MODEL IND1_1 IND (L=900M)

Now the circuit that violates the specification can be edited and simulated directly so a solution may be found for the violation.

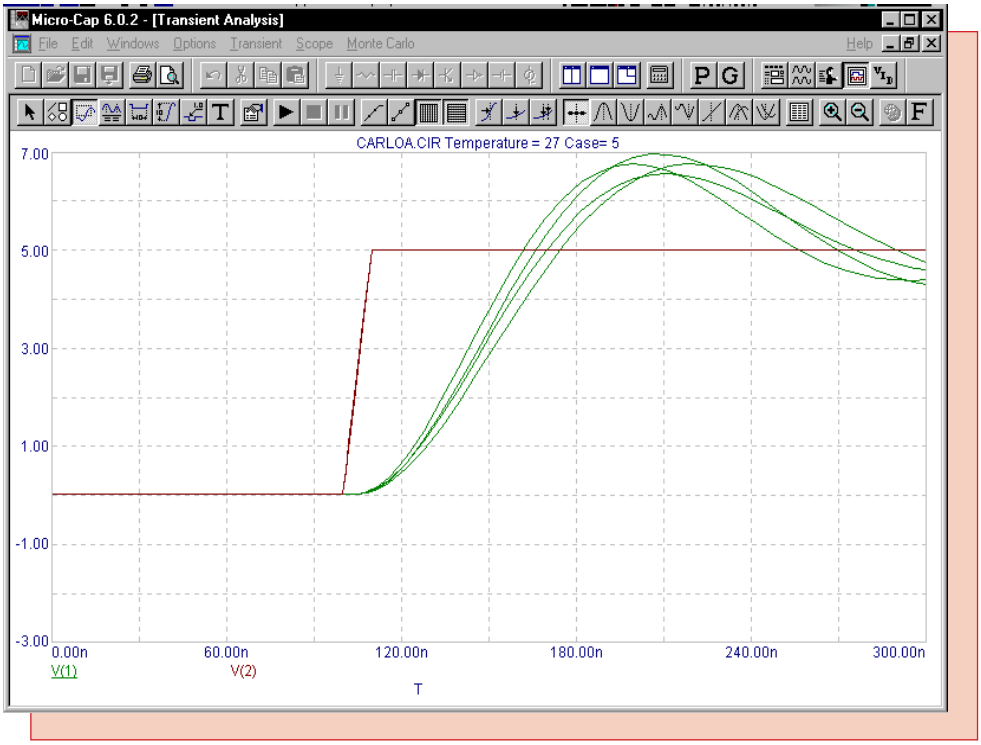


Fig. 8 - Monte Carlo Transient Analysis Results

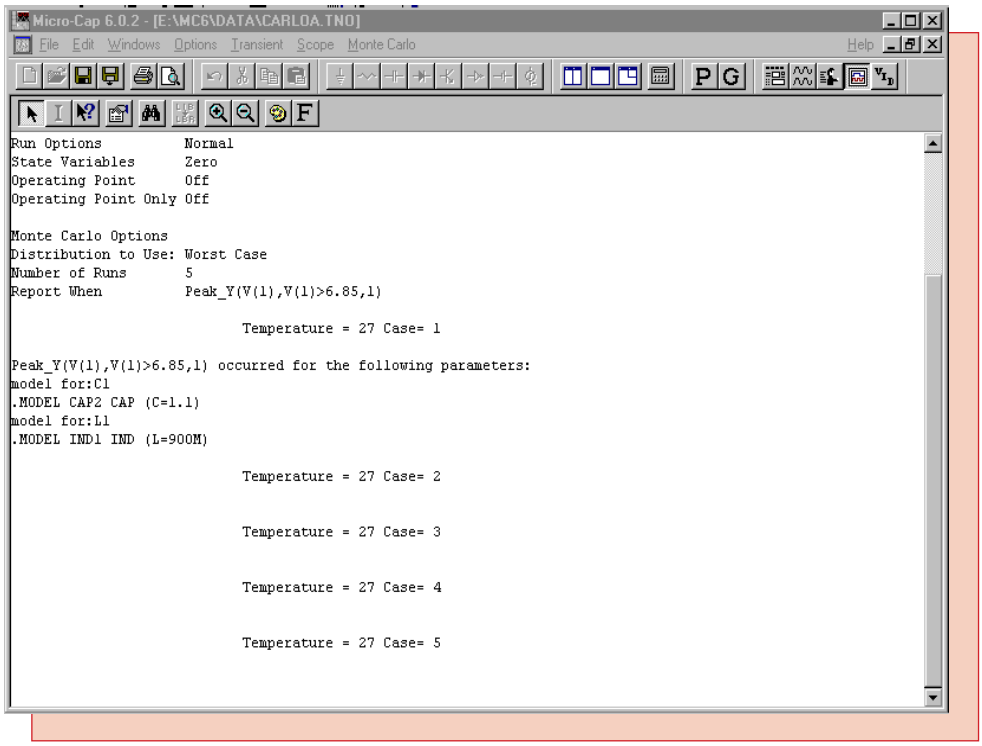


Fig. 9 - Monte Carlo Error Report in the Numeric Output

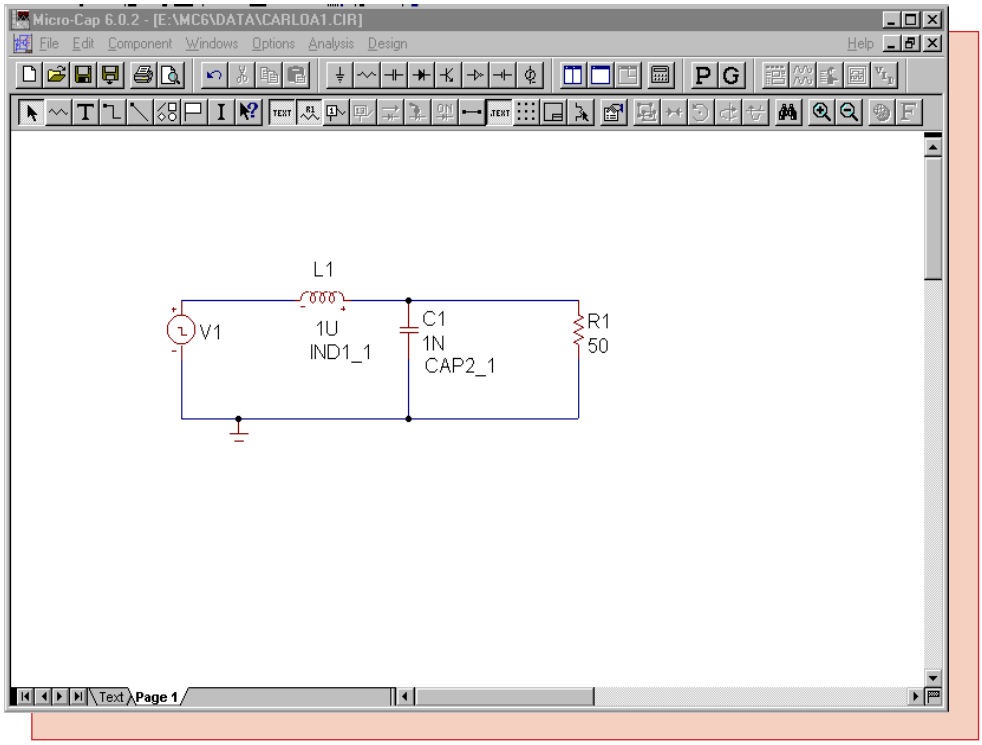


Fig. 10 - Loaded Monte Carlo Schematic File

NTC7 Test Signal

Video testing is performed by placing a known test signal at the input of the system and observing the output to see if there is any distortion. If the system can pass the signal with little or no distortion, then it will be able to pass a picture signal as well. One such test signal is the NTC7 composite test signal. The NTC7 signal provides a user with multiple video-system testing opportunities. The white bar is used for testing insertion gain and distortions in medium time waveforms. The 2T pulse is used for testing distortions in short-time waveforms. The 12.5T pulse tests for luminance-chrominance delay disparities. Finally, the modulated staircase tests the differential gain and differential phase errors.

To create this signal in Micro-Cap, multiple voltage sources must be used. The schematic in Figure 11 displays one configuration of sources that can be used to create the NTC7 test signal. This configuration was created based on an article by Anthony Radice, titled "Spice Simulations Use

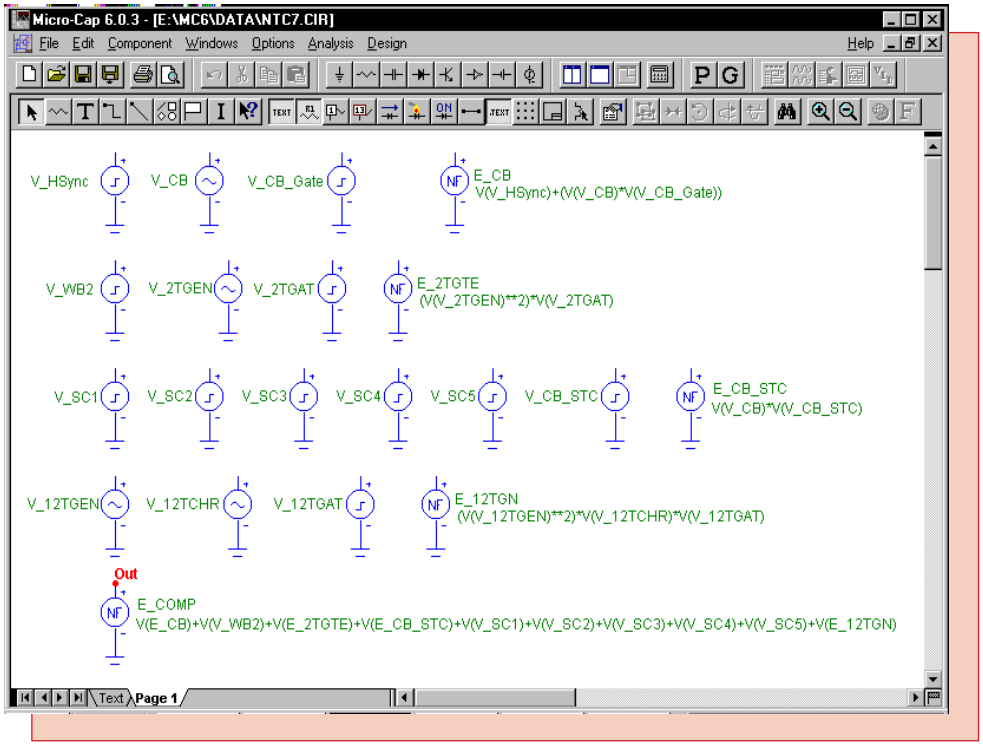


Fig. 11 - NTC7 Test Signal Macro

Controlled Sources to Model NTSC Signals" which appeared in the March 1, 1991 issue of EDN. This schematic can easily be turned into a macro for use in other schematics.

Note that for all of the following sources that use model statements, both the PART attribute and the MODEL attribute have been defined with the same name, and that the period for the NTC7 test signal is assumed to be 63.56us. For this signal, volts represent IRE levels. 0V would be the blank level (0 IRE) and 1V would be the white level (100 IRE). The negative going horizontal sync pulse is created by the V_HSync pulse source. This source uses the following model statement:

.MODEL V_HSYNC PUL (VONE=-0.4 P1=1.4u P2=1.6u P3=6.3u P4=6.5u P5=63.56u)

The model creates -0.4V pulse with 0.2us rise and fall times and a width of 4.7us. Otherwise, the

voltage level of the pulse will be zero volts. The color-burst signal is created from a combination of the V_CB sine source and the V_CB_Gate pulse source. This signal refers to 9 cycles of a 3.58MHz subcarrier that provides a reference for the color phase and the color saturation level. The V_CB sine source creates a sine wave with a 0.2V peak amplitude and a frequency of 3,579,545Hz, and the V_CB_Gate pulse source produces a 1V pulse for 2.6us starting at 7.2us. These sources use the following model statements:

```
.MODEL V_CB SIN (F=3579545 A=.2)
.MODEL V_CB_GATE PUL (VONE=1 P1=7u P2=7.2u P3=9.8u P4=10u P5=63.56u)
```

The nonlinear fuction voltage source, E_CB, then proceeds to multiply the V_CB and V_CB_Gate signals together. When multiplied, the pulse source zeroes out the sine source for all but the 2.6us where the pulse source has a value of 1V. This gates the sine source generator and produces the appropriate color burst. In addition to producing the color bust, the E_CB function source also adds the horizontal sync and the color burst together. The entire VALUE attribute for the E_CB source is:

```
V(V_HSync)+(V(V_CB)*V(V_CB_Gate))
```

The white bar is created by the V_WB2 pulse source. This source creates a 1V (100 IRE) pulse that starts at 13.6us and lasts for 18us. For the rest of the signal, it is at 0V. The V_WB2 source uses the model statement:

```
.MODEL V_WB2 PUL (VONE=1 P1=13.4u P2=13.6u P3=31.6u P4=31.8u P5=63.56u)
```

The 2T pulse is created from a combination of the V_2TGEN sine source, the V_2TGAT pulse source, and the E_2TGTE function source. The 2T pulse has a $\sin^2$ characteristic and a pulse width equal to two periods of the 3.58MHz chroma subcarrier which is used in the color burst. This characteristic can be simulated by squaring a 1V sine source that has a frequency of 894,886Hz. Squaring the sine source produces voltage levels between 0V and 1V at a frequency of 1.79MHz. The peak of this pulse should be centered on 35.4us. In order to do this, the sine source must have a phase shift. For the center to be at this time, the sine source must be crossing 0V at exactly 35.1255us. Since one period of the sine source is 1.117us, the phase shift for the sine source can then be calculated to be 244 degrees. The V_2TGAT pulse source then gates the V_2TGEN sine source by simulating a 1V pulse starting at 35.1265us for .559us which covers exactly one period of the squared sine source. The two model statements used by these sources are:

```
.MODEL V_2TGEN SIN (F=894886 PH=3.543)
.MODEL V_2TGAT PUL (VONE=1 P1=35.1255u P2=35.1265u P3=35.6835u P4=35.6845u
+ P5=63.56u)
```

Note that the phase parameter in the sine source has been converted into its radian equivalent. The E_2TGTE function voltage source is used to square the sine source and then multiply the result by the gating pulse source to produce the 2T pulse. The VALUE attribute for the E_2TGTE source is defined as:

```
(V(V_2TGEN)**2)*V(V_2TGAT)
```

The 12.5T modulated pulse is created from a combination of the V_12TGEN sine source, the

V_12TCHR sine source, the V_12TGAT pulse source, and the E_12TGN function source. This pulse has a $\sin^2$ characteristic and a width equal to 12.5 periods of the 3.58MHz chroma subcarrier. The envelope of this pulse is created in the same manner as the 2T pulse where, in this case, a 1V sine source with a frequency of 143,182Hz is squared to produce the 0V to 1V amplitude and a frequency of 286,364Hz. The peak of the 12.5T pulse should be centered at 38.4us so a phase shift for the sine source needs to be calculated. Since the period of the sine source is 3.492us and the zero crossing must occur at 36.654us, then the phase can be calculated to be 89 degrees. The modulating sine source for the 12.5T pulse is a 3.58MHz sine souce. Since the source should be between 0 IRE (0V) and 100 IRE (1V), both the DC component and the amplitude of this source should be set to .5V. The V_12TGAT pulse source is used to gate the pulse. It produces a 1V pulse starting at 36.655us that will last for 3.49us. The model statements for these three sources are as follows:

```
.MODEL V_12TGEN SIN (F=143182 PH=1.553343)
.MODEL V_12TCHR SIN (F=3579545 A=.5 DC=.5)
.MODEL V_12TGAT PUL (VONE=1 P1=36.654u P2=36.655u P3=40.145u P4=40.146u
+ P5=63.56u)
```

Again, the phase for the sine source has been converted into its radian equivalent. The E_12TGN function source is then used to square the V_12TGEN signal and multiply the result by the two other sources to produce the final 12.5T modulated pulse. The VALUE attribute for this source is defined as:

```
(V(V_12TGEN)**2)*V(V_12TCHR)*V(V_12TGAT)
```

The last stage of this signal is the modulated staircase. This portion of the signal can be regarded as six bursts of the chroma that was also used for the color burst. The center for each step of the staircase is 18 IRE (.18V) higher than the previous step, rising to a maximum of 90 IRE (.9V) with the sixth step. The staircase is created from a combination of the V_CB sine source, the V_SC1 to V_SC5 pulse sources, the V_CB_STC pulse source, and the E_CB_STC function source. Since the phase of the chroma should be 0 degrees and the amplitude .2V, the chroma can be taken from the V_CB sine source which was described earlier in the article. This source provides the modulation for the staircase. The V_SC1 to V_SC5 pulse sources provide the center voltage for each of the steps in the staircase. The modulated staircase has six steps, but since the first step is centered around 0V, only five pulse sources are needed. Note that the timing of the pulse sources overlap each other so that there is an additive effect on the base level of the chroma signal. Each pulse source has an amplitude of .18V and occurs 3us after the previous step began thus creating the staircase effect. The V_CB_STC pulse source provides a gating signal for the V_CB chroma signal. It produces a 1V pulse starting at 43.4us and lasting for the entire 19us that the modulated staircase lasts for. The model statements for all of these pulse sources are as follows:

```
.MODEL V_SC1 PUL (VONE=.18 P1=47.4u P2=47.41u P3=62.41u P4=62.42u P5=63.56u)
.MODEL V_SC2 PUL (VONE=.18 P1=50.4U P2=50.41U P3=62.41U P4=62.42U P5=63.56U)
.MODEL V_SC3 PUL (VONE=.18 P1=53.4U P2=53.41U P3=62.41U P4=62.42U P5=63.56U)
.MODEL V_SC4 PUL (VONE=.18 P1=56.4U P2=56.41U P3=62.41U P4=62.42U P5=63.56U)
.MODEL V_SC5 PUL (VONE=.18 P1=59.4U P2=59.41U P3=62.41U P4=62.42U P5=63.56U)
.MODEL V_CB_STC PUL (VONE=1 P1=43.4u P2=43.41u P3=62.41u P4=62.42u
+P5=63.56u)
```

The E_CB_STC function source is then used to multiply the V_CB chroma signal and the V_CB_STC gate signal which zeroes out the chroma signal except for the 19us needed for the

staircase. The VALUE attribute defined for the function source is:

V(V_CB)*V(V_CB_STC)

Finally, the E_COMP function source is used to add all of the different components of the NTC7 composite signal together. The VALUE attribute for this source is defined as:

V(E_CB)+V(V_WB2)+V(E_2TGTE)+V(E_CB_STC)+V(V_SC1)+V(V_SC2)+V(V_SC3)
+V(V_SC4)+V(V_SC5)+V(E_12TGN)

The + sign that begins the second line above is not a continuation character in this case but is actually used for addition.

The final simulation result of the NTC7 composite signal is displayed in Figure 12. Since the signal is dependent on phase shifts to produce the 2T and the 12.5T pulses, it is only reliable over a single period of simulation.

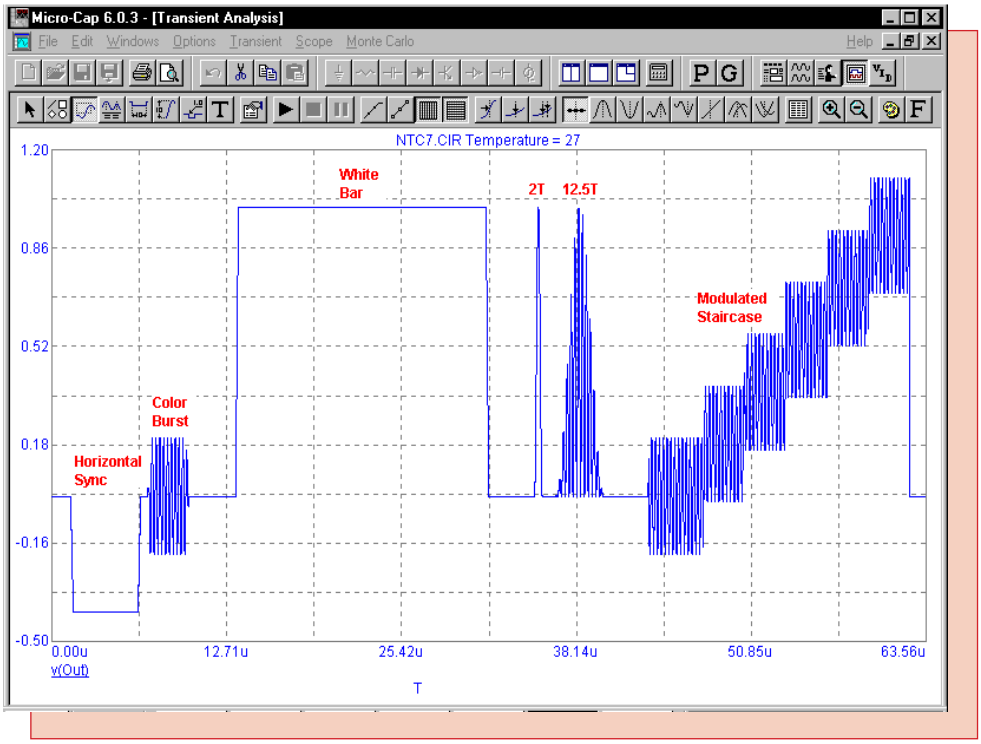


Fig. 12 - NTC7 Test Signal

Product Sheet

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